Josep Torrellas

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Education

Aug 92	Ph.D. in Electrical Engineering, Stanford University. Dissertation: "Multiprocessor Cache Memory Performance: Characterization and Optimization". Advisor: John Hennessy.
Dec 87	M.S. in Electrical and Computer Engineering, University of Wisconsin - Madison.
Jun 86	B.S. in Electrical Engineering, Universitat Politecnica de Catalunya, Spain.

Appointments

Aug 20	-	pres.	Professor, Coordinated Science Laboratory (CSL), University of Illinois at Urbana-Champaign (UIUC).
Jun 18	-	pres.	Co-Leader, Intel Strategic Research Alliance (ISRA) Center on Computer Security, UIUC.
Jan 16	-	pres.	Saburo Muroga Professor of Computer Science, UIUC.
Jan 11	-	pres.	Director, Center for Programmable Extreme-Scale Computing, UIUC.
Sep 11	-	Sep 13	Director, Illinois-Intel Parallelism Center (I2PC), UIUC.
Jan 06	-	pres.	Researcher, Information Trust Institute (ITI), UIUC.
Aug 02	-	pres.	Professor, Computer Science Department, UIUC.
Aug 02	-	Aug 09	Willett Faculty Scholar, Computer Science Department, UIUC.
Sep 07	-	Aug 10	Leader, University of Illinois OpenSPARC Center of Excellence, UIUC.
Feb 08	-	Aug 11	Computer Architecture Leader, Universal Parallel Computing Research Center (UPCRC), UIUC.
Aug 98	-	Aug 02	Associate Professor, Computer Science Department, UIUC.
May 98	-	Jan 99	Research Staff Member, IBM T.J. Watson Research Center, IBM Research (sabbatical).
Apr 93	-	pres.	Departmental Affiliate, Electrical and Computer Engineering Department, UIUC.
Aug 92	-	Aug 98	Assistant Professor, Computer Science Department, UIUC.
Sep 92	-	Dec 96	Senior Computer Systems Engineer, Center for Supercomp. Research and Develop. (CSRD), UIUC.

Honors & Awards

2021	First Prize, Intel Hardware Security Academic Award, for the paper "Speculative Data-Oblivious Execution: Mobilizing Safe Prediction For Safe and Efficient Speculative Execution".
2021	IEEE Computer Society Harry H. Goode Memorial Award. For "Contributions to energy efficient and programmable shared-memory multiprocessor architectures".
2021	In List of Teachers Ranked as Excellent by their Students: Spring 2021.
2021	One Selected paper and one Honorable Mention paper in 2021 IEEE Micro Top Picks from Computer Architecture Conferences.
2020	Upstreamed to Linux 5.11 the *Draco* System Call checking software.
2020	Best Paper Award, International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2020.
2020	Two Selected papers and one Honorable Mention paper in 2020 IEEE Micro Top Picks from Computer Architecture Conferences.
2020	Google Faculty Research Award.
2020	Keynote at the 2020 HPCA/PPoPP/CGO conferences.
2020	Research Highlight paper in Communications of the ACM (CACM).
2020	Cover article in IEEE Control Systems Magazine.
2019	In List of Teachers Ranked as Excellent by their Students: Spring 2019 and Fall 2019.
2019	Best Paper Award, 52nd International Symposium on Microarchitecture (MICRO), October 2019.

2019 Honorable Mention Paper, 2019 IEEE Micro Top Picks from Computer Architecture Conferences.
2018 Co-Leader, Intel Strategic Research Alliance (ISRA) Center on Computer Security.
2018 In List of Teachers Ranked as Excellent by their Students: Spring 2018 and Fall 2018.
2017 Best Paper Nominee, International Conference on Parallel Architectures and Compilation Techniques (PACT).
2017 University of Illinois at Urbana-Champaign Campus Award for Excellence in Graduate Student Mentoring.
2016 Fellow of the American Association for the Advancement of Science (AAAS).
2016 Member of the Board of Directors (Elected), Computing Research Association (CRA).
2016 Saburo Muroga Professorship of Computer Science, UIUC.
2015 IEEE Computer Society Technical Achievement Award. For "Pioneering contributions to shared-memory multiprocessor architectures and thread-level speculation".
2015 Honorable Mention Paper, 2015 IEEE Micro Top Picks from Computer Architecture Conferences.
2014 Distinguished Paper Award, International Conference on Programming Language Design and Implementation (PLDI), June 2014.
2014 Best Paper Award Finalist, International Symposium on High Performance Computer Architecture (HPCA), Feburary 2014.
2013 Distinguished Speaker Award, IEEE International Conference on Application Specific Systems, Architectures and Processors (ASAP), June 2013.
2012 High-Impact Paper Award, International Conference on Computer Design (ICCD), October 2012. For "One of the 5 most cited papers in the first 30 years of ICCD (1983-2012)".
2012 Jon Postel Distinguished Lecturer, Computer Science Department, UCLA, November 2012.
2011 Council Member, The Computing Community Consortium (CCC), CRA.
2010 ACM Fellow.
2009 Best Paper Award, 42nd International Symposium on Microarchitecture (MICRO), December 2009.
2009 Paper in 2009 IEEE Micro's Top Picks from Computer Architecture Conferences.
2009 Research Highlight paper in Communications of the ACM (CACM).
2009 Best Idea Award, Wild and Crazy Ideas Session, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2009.
2007 Paper in 2007 IEEE Micro's Top Picks from Computer Architecture Conferences.
2006 Best Paper Award, 39th International Symposium on Microarchitecture (MICRO), December 2006.
2006 Paper in 2006 IEEE Micro's Top Picks from Computer Architecture Conferences.
2004 Paper in 2004 IEEE Micro's Top Picks from Computer Architecture Conferences.
2004 IEEE Fellow.
2003 Paper in 2003 IEEE Micro's Top Picks from Computer Architecture Conferences.
2002-9 Willett Faculty Scholar, UIUC.
2001 Best Paper Award, Fifth Workshop on Multithreaded Execution, Architecture, and Compilation.
2000 Senior Xerox Award for Outstanding Faculty Research, UIUC.
1997-00 IBM Partnership Award.
1997 C. W. Gear Outstanding Junior Faculty Award, UIUC.
1997 Junior Xerox Award for Outstanding Faculty Research, UIUC.
1995,6,8 Intel Research Council Award.
1994-9 Young Investigator Award, National Science Foundation.
1993-6 Research Initiation Award, National Science Foundation.

Main Professional Service

Nov 18 - pres. Chair, The Institute of Electrical and Electronics Engineers (IEEE) Technical Committee on Computer Architecture (TCCA). Main activities include:
– Help organize and fund over 10 technical conferences yearly
– Promote the careers of members
– Co-ordinate many activities for the betterment of the computer architecture community
– Provide funds for students to travel to conferences
– Serve in the Steering Committees of conferences

May 18 - pres. Member, U.S. National Academies Board on Army Research and Development.
– Co-organizer, workshops on "Machine Learning and High-Performance Computing", May 2020 and August 2020.

Mar 18	Co-organizer, NSF Visioning Workshop on "Inter-Disciplinary Research Challenges in Computer Systems for the 2020s", Williamsburg, VA. Workshop produced a report that was handed over to NSF and was published in the ACM Digital Library.
Sep 16 - pres.	Member, International Roadmap for Devices and Systems (IRDS) Applications Benchmarking Focus Team. – Successor of International Technology Roadmap for Semiconductors.
Jul 16 - Jun 19	Member, Board of Directors, Computing Research Association (CRA). Main activities included: – Co-lead an initiative to improve computer science faculty recruiting by creating an on-line CRA database of faculty candidates. – Co-organize a session on "Improving Faculty Recruiting in the Computing Community" in the 2018 Conference at Snowbird, July 2018.
Apr 15	Attendee, Leadership in Science Policy Institute Workshop, Computing Community Consortium (CCC), Washington DC.
Jan 11 - Jun 14	Council Member, The Computing Community Consortium (CCC), CRA. Main activities included: – Member of the Subcommittee on Visioning Activities – Laision for a visioning workshop by the design automation community
June 13	Chair and co-editor, "SIGARCH/TCCA's Recommended Best Practices for ISCA Program Chairs".
May 12	Co-editor, CCC Visioning white paper: "21st Century Computer Architecture, A Community White Paper".
Oct 10 - Oct 18	Member of the Executive Committee, IEEE TCCA.
Jul 05 - Oct 10	Chair, IEEE TCCA. Main accomplishments included: – Successfully co-located ACM PPoPP and IEEE HPCA for interdisciplinary interactions – Created the HPCA Hall of Fame and the HPCA Conference Repository – Created the HPCA conference Industrial Session – Distributed hard copies of HPCA proceedings
Feb 10 - Sep 10	Co-organizer of two CCC Visioning Workshops on Advancing Computer Architecture Research: "Failure is not an Option: Popular Parallel Programming" and "What Now in ILP Research?".
Dec 05	Participant in the CRA Visioning workshop: "Revitalizing Computer Architecture Research".
Jul 98 - Jul 05	Vice-Chair and Member of the Advisory Board, IEEE TCCA.

Designed Architectures

1. *QuickRec: A Hardware Prototype for Recording and Deterministically Replaying Multithreaded Programs in the Intel Architecture.* This prototype has been developed in collaboration with Intel, and is described in the QuickRec ISCA-2013 paper: http://iacoma.cs.uiuc.edu/iacoma-papers/isca13_1.pdf.

2. *Runnemede: An Chip Multiprocessor for Extreme-Scale Computing.* This manycore chip has been designed in collaboration with Intel, and is described in the Runnemede HPCA-2013 paper: http://iacoma.cs.uiuc.edu/iacoma-papers/hpca13_1.pdf.

Designed Software

1. *DRACO: A Linux Patch to Speed-up System Call Checking*. This is a patch in the official Linux distribution that checks system calls for security. December 2020.

2. *VARIUS and VARIUS-NTV: A Model of Process Variation*. This tool models within-die process variation and the resulting timing errors in manycores at a level suitable for microarchitects. June 2007. http://iacoma.cs.uiuc.edu/varius/index.html.

3. *SESC: A Simulator of Superscalar Multiprocessors and Memory Systems with Thread-Level Speculation Support*. SESC is a multiprocessor simulator package with support for thread-level speculation. June 2005. http://sourceforge.net/projects/sesc.

4. *Scal-Tool: Pinpointing and Quantifying Scalability Bottlenecks in DSM Multiprocessors*. Scal-Tool is a public-domain tool that is available through the NCSA software repository. May 1999.

5. *Augmint: A Multiprocessor Simulation Environment for Intel x86 Architectures*. Augmint is a multiprocessor tracing and evaluation package that runs on Intel x86 machines. December 1995. http://iacoma.cs.uiuc.edu/augmint.html.

Graduated 43 Ph.D. Students (15 are Faculty at Top US Universities)

1. Dimitrios Skarlatos, 2020. First Job: Assistant Professor, Department of Computer Science, Carnegie Mellon University, Pittsburgh, PA. Thesis: "Rethinking Computer Architecture and Operating System Abstractions for Good and Evil".

2. Raghavendra Pothukuchi, 2020. First Job: Postdoctoral Researcher, Department of Computer Science, Yale University. Thesis: "Intelligent Systems for Efficiency and Security".

3. Thomas Shull, 2020. First Job: Senior Member of Technical Staff, Oracle Labs, Zurich, Switzerland. Thesis: "Making Non-Volatile Memory Programmable".

4. Yasser Shalabi, 2020. First Job: Symmetry Systems. Thesis: "Leveraging Concurrency for Performance and Security".

5. Mengjia Yan, 2019. First Job: Assistant Professor, Department of Electrical Engineering and Computer Science, MIT, MA. Thesis: "Cache-Based Side Channels: Modern Attacks and Defenses". David J. Kuck Outstanding PhD Thesis Award. Also, Honorable Mention of the 2020 ACM SIGARCH/IEEE CS TCCA Outstanding Dissertation Award.

6. Bhargava Gopireddy, 2018. First Job: Nvidia, Santa Clara, CA. Thesis: "Energy Efficient Core Designs For Upcoming Process Technologies".

7. Jiho Choi, 2018. First Job: Google, Mountain View, CA. Thesis: "HW-SW Co-Design Techniques For Modern Programming Languages".

8. Wooil Kim, 2015. First Job: Member of Technical Staff, Samsung Electronics, Seoul, Korea. Thesis: "Architecting, Programming, and Evaluating an On-Chip Incoherent Multiprocessor Memory Hierarchy".

9. Nima Honarmand, 2014. First Job: Assistant Professor, Department of Computer Science, Stony Brook University, Stony Brook, NY. Thesis: "Record and Deterministic Replay of Parallel Programs on Multiprocessors".

10. Aditya Agrawal, 2014. First Job: Member of Research Staff, NVidia, Santa Clara, CA. Thesis: "Refresh Reduction in Dynamic Memories".

11. Yuelu Duan, 2014. First Job: Member of Technical Staff, VMware, San Diego, CA. Thesis: "Techniques for Low Overhead Fences and Sequential Consistency Violation Recording".

12. Xuehai Qian, 2013. Current Job: Assistant Professor, Department of Electrical Engineering, University of Southern California, Los Angeles, CA. Thesis: "Scalable and Flexible Bulk Architecture".

13. Shanxiang Qi, 2013. First Job: Member of Technical Staff, Google, Mountain View, CA. Thesis: "Techniques to Detect and Avert Advanced Software Concurrency Bugs".

14. Ulya Karpuzcu, 2012. First Job: Assistant Professor, Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN. Thesis: "Novel Many-Core Architectures for Energy-Efficiency".

15. Abdullah Muzahid, 2012. Current Job: Assistant Professor, Department of Computer Science and Engineering, Texas A&M University, College Station, TX. Thesis: "Effective Architectural Support For Detecting Concurrency Bugs".

16. Daniel Wonsun Ahn, 2012. Current Job: Assistant Professor, Department of Computer Science, University of Pittsburgh, Pittsburgh, PA. Thesis: "Software and Architecture Support for the BULK Multicore".

17. Pablo Montesinos, 2009. First Job: Member of Research Staff, Samsung Laboratories, San Jose, CA. Thesis: "Practical Time Travel of Multiprocessor Systems".

18. Brian Greskamp, 2009. First Job: Member of Research Staff, D. E. Shaw Research, New York, NY. Thesis: ”Improving Per-Thread Performance on CMPs through Timing Speculation”.

19. Radu Teodorescu, 2008. First Job: Assistant Professor, Department of Computer Science and Engineering, Ohio State University, Columbus, OH. Thesis: ”Multilayer Techniques to Address Parameter Variation”.

20. Abhishek Tiwari, 2008. First Job: Member of Technical Staff, Goldman Sachs, New York, NY. Thesis: ”Architectural Techniques to Mitigate the Effect of Spatial and Temporal Variations in Processors”.

21. Luis Ceze, 2007. First Job: Assistant Professor, Department of Computer Science and Engineering, University of Washington, Seattle, WA. Thesis: ”Bulk Operation and Data Coloring for Multiprocessor Programmability”.

22. James Tuck, 2007. First Job: Assistant Professor, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC. Thesis: ”Efficient Support for Speculative Tasking”.

23. Karin Strauss, 2007. First Job: Member of Research Staff, AMD Laboratories, Seattle, WA. Thesis: ”Cache Coherence in Embedded-Ring Multiprocessors”.

24. Smruti R. Sarangi, 2007. Current Job: Assistant Professor, Department of Computer Science and Engineering, Indian Institute of Technology, New Delhi, India. Thesis: ”Techniques to Mitigate the Effects of Congenital Faults in Processors”.

25. Jun Nakano, 2006. First Job: Member of Research Staff, IBM Research, Tokyo, Japan. Thesis: ”Techniques to Address Unreliability and Variability of Computing Systems”.

26. Jose Renau, 2004. First Job: Assistant Professor, Department of Computer Engineering, University of California, Santa Cruz. Thesis: ”Chip Multiprocessors with Speculative Multithreading: Design for Performance and Energy Efficiency”.

27. Milos Prvulovic, 2003. First Job: Assistant Professor, College of Computing, Georgia Institute of Technology, Atlanta, GA. Thesis: ”Architectural Support for Reliable Parallel Computing”.

28. Jose Martinez, 2002. First Job: Assistant Professor, Department of Electrical and Computer Engineering, Cornell University, Ithaca, NY. Thesis: ”Speculative Shared-Memory Architectures”.

29. Yan Solihin, 2002. First Job: Assistant Professor, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC. Thesis: ”Improving Memory Performance Using Intelligent Memory”.

30. Michael Huang, 2002. First Job: Assistant Professor, Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY. Thesis: ”Managing Processor Adaptation for Energy Reduction and Temperature Control”.

31. Anthony Nguyen, 2002. Current Job: Member of Research Staff, Intel Corporation, Santa Clara, CA. Thesis: ”High-Throughput Coherence Controllers”.

32. Marcelo Cintra, 2001. First Job: Lecturer, School of Informatics, University of Edinburgh, UK. Thesis: ”Architectural Support for Scalable Speculative Parallelization in Shared-Memory Multiprocessors”.

33. Seung-Moon Yoo, 2001. First Job: Member of Research Staff, IBM Research, Austin, TX. Thesis: ”Design of Energy-Efficient SOCs with Deep Sub-Micron Circuit Techniques”.

34. Qiang Cao, 2000. First Job: Member of Technical Staff, Oracle Corporation, Redwood Shores, CA. Thesis: ”Performance Characterization and Buffer Memory Optimization of Databases”.

35. Sujoy Basu, 2000. First Job: Member of Research Staff, Hewlett-Packard Laboratories, Palo Alto, CA. Thesis: ”Design of Efficient Simple COMA Architectures”.

36. Yi Kang, 1999. First Job: Microprocessor Design Group, Sun Microsystems, Menlo Park, CA. Thesis: ”An Intelligent Memory for Data Intensive Applications”.

37. Ye Zhang, 1999. First Job: Member of Technical Staff, Oracle Corporation, Redwood Shores, CA. Thesis: "Speculative Parallelization in DSM Multiprocessors".

38. Pedro Trancoso, 1998. Current Job: Lecturer, Department of Computer Science, University of Cyprus, Cyprus. Thesis: "Optimizing Memory-Resident DSS Workloads for Caches".

39. Venkata Krishnan, 1998. First Job: Microprocessor Design Group, DEC Shrewsbury, MA. Thesis: "Speculative Multithreading Architectures".

40. Liuxi Yang, 1997. First Job: Microprocessor Design Group, Sun Microsystems, Menlo Park, CA. Thesis: "Using Advanced Memory Technologies to Build DSM Multiprocessors".

41. David Koufaty, 1997. First Job: Member of Technical Staff, Intel Corp, Hillsboro, OR. Thesis: "Compiler Support to Hide Coherence Misses in Shared-Memory Multiprocessors".

42. Zheng Zhang, 1996. First Job: Member of Research Staff, Hewlett-Packard Laboratories, Palo Alto, CA. Thesis: "Design Alternatives to Reduce Remote Conflict Misses in Shared-Memory Multiprocessors".

43. Chun Xia, 1996. First Job: Member of Technical Staff, Sun Microsystems, Menlo Park, CA. Thesis: "Exploiting Multiprocessor Memory Hierarchies for Operating Systems".

Publications. Conferences

1. Raghavendra Pothukuchi, Sweta Pothukuchi, Petros Voulgaris, Alex Schwing, Josep Torrellas, *Maya: Using Formal Control to Obfuscate Power Side Channels*, International Symposium on Computer Architecture (ISCA), June 2021.

2. Thomas Shull, Nikos Nikoleris, Ilias Vougioukas, Wendy Elsasser, Josep Torrellas, *Execution Dependence Extension (EDE): ISA Support for Eliminating Fences*, International Symposium on Computer Architecture (ISCA), June 2021.

3. Daixuan Li, Benjamin Reidys, Jinghan Sun, Thomas Shull, Josep Torrellas, Jian Huang, *UniHeap: Managing Persistent Objects Across Managed Runtimes for Non-Volatile Memory*, International Systems and Storage Conference (SYSTOR), June 2021.

4. Dimitrios Skarlatos, Zirui Neil Zhao, Riccardo Paccagnella, Christopher Fletcher, Josep Torrellas, *Jamais Vu: Thwarting Microarchitectural Replay Attacks*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April 2021.

5. M. Behnia, P. Sahu, R. Paccagnella, J. Yu, Z. Zhao, X. Zou, T. Unterluggauer, J. Torrellas, C. Rozas, A. Morrison, F. Mckeen, F. Liu, R. Gabor, C. Fletcher, A. Basak, A. Alameldeen, *Speculative Interference Attacks: Breaking Invisible Speculation Schemes*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April 2021.

6. Suraj Jog, Zikun Liu, Antonio Franques, Vimuth Fernando, Sergi Abadal, Josep Torrellas, Haitham Hassanieh, *One Protocol to Rule Them All: Deep Reinforcement Learning Aided MAC for Wireless Network-on-Chips*, USENIX Symposium on Networked Systems Design and Implementation (NSDI), April 2021.

7. Antonio Franques, Sergi Abadal, Haitham Hassanieh, Josep Torrellas, *Fuzzy-Token: An Adaptive MAC Protocol for Wireless-Enabled Manycores*, Design, Automation and Test in Europe Conference (DATE), February 2021.

8. Antonio Franques, Apostolos Kokolis, Sergi Abadal, Vimuth Fernando, Sasa Misailovic, and Josep Torrellas, *WiDir: A Wireless-Enabled Directory Cache Coherence Protocol*, International Symposium on High-Performance Computer Architecture (HPCA), February 2021.

9. Zirui Neil Zhao, Houxiang Ji, Mengjia Yan, Jiyong Yu, Christopher W. Fletcher, Adam Morrison, Darko Marinov, and Josep Torrellas, *Speculation Invariance (InvarSpec): Faster Safe Execution Through Program Analysis*, International Symposium on Microarchitecture (MICRO), October 2020.

10. Apostolos Kokolis, Thomas Shull, Jian Huang, and Josep Torrellas, *P-INSPECT: Architectural Support for Programmable Non-Volatile Memory Frameworks*, International Symposium on Microarchitecture (MICRO), October 2020.

11. Zhangxiaowen Gong, Houxiang Ji, Christopher W. Fletcher, Christopher J. Hughes, Sara Baghsorkhi, and Josep Torrellas, *SAVE: Sparsity-Aware Vector Engine for Accelerating DNN Training and Inference on CPUs*, International Symposium on Microarchitecture (MICRO), October 2020.

12. Dimitrios Skarlatos, Qingrong Chen, Jianyan Chen, Tianyin Xu, and Josep Torrellas, *Draco: Architectural and Operating System Support for System Call Security*, International Symposium on Microarchitecture (MICRO), October 2020.

13. Serif Yesil, Azin Heidarshenas, Adam Morrison, and Josep Torrellas, *Speeding Up SpMV for Power-Law Graph Analytics by Enhancing Locality and Vectorization*, International Conference for High Performance Computing, Networking, Storage, and Analysis (SC), November 2020.

14. Zhangxiaowen Gong, Houxiang Ji, Christopher W. Fletcher, Christopher J. Hughes, and Josep Torrellas, *SparseTrain: Leveraging Dynamic Sparsity in Software for Training DNNs on General-Purpose SIMD Processors*, International Conference on Parallel Architectures and Compilation Techniques (PACT), October 2020.

15. Mengjia Yan, Christopher W. Fletcher, and Josep Torrellas, *Cache Telepathy: Leveraging Shared Resource Attacks to Learn DNN Architectures*, USENIX Security Symposium (USS), August 2020.

16. Dimitrios Skarlatos, Umur Darbaz, Bhargava Gopireddy, Nam Sung Kim, and Josep Torrellas, *BabelFish: Fusing Address Translations for Containers*, International Symposium on Computer Architecture (ISCA), June 2020. **Selected as Top Picks from Computer Architecture Conferences.**

17. Jiyong Yu, Namrata Mantri, Josep Torrellas, Adam Morrison, and Christopher W. Fletcher, *Speculative Data-Oblivious Execution: Mobilizing Safe Prediction For Safe and Efficient Speculative Execution*, International Symposium on Computer Architecture (ISCA), June 2020. **Selected as First Prize in Intel Hardware Security Academic Award.**

18. Azin Heidarshenas, Tanmay Gangwani, Serif Yesil, Adam Morrison, and Josep Torrellas, *SNUG: Architectural Support for Relaxed Concurrent Priority Queueing in Chip Multiprocessors*, International Conference on Supercomputing (ICS), June 2020.

19. Azin Heidarshenas, Serif Yesil, Dimitrios Skarlatos, Sasa Misailovic, Adam Morrison and Josep Torrellas, *V-Combiner: Speeding-up Iterative Graph Processing on a Shared-Memory Platform with Vertex Merging*, International Conference on Supercomputing (ICS), June 2020.

20. Dimitrios Skarlatos, Apostolos Kokolis, Tianyin Xu, and Josep Torrellas, *Elastic Cuckoo Page Tables: Rethinking Virtual Memory Translation for Parallelism*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2020. **ASPLOS 2020 Best Paper Award.** Also **Selected as an Honorable Mention in IEEE Micro Top Picks from Computer Architecture Conferences.**

21. Raghavendra Pradyumna Pothukuchi, Joseph L. Greathouse, Karthik Rao, Christopher Erb, Leonardo Piga, Petros Voulgaris, and Josep Torrellas, *Tangram: Integrated Control of Heterogeneous Computers*, International Symposium on Microarchitecture (MICRO), October 2019.

22. Jiyong Yu, Mengjia Yan, Artem Khyzha, Adam Morrison, Josep Torrellas, and Christopher Fletcher, *Speculative Taint Tracking (STT): A Comprehensive Protection for Speculatively Accessed Data*, International Symposium on Microarchitecture (MICRO), October 2019. **MICRO 2019 Best Paper Award.** Also **selected as a IEEE Micro 2020 Top Pick from Computer Architecture Conferences.** Also **Research Highlight, Communications of the ACM (CACM).**

23. Serif Yesil, Azin Heidarshenas, Adam Morrison, and Josep Torrellas, *Understanding Priority-Based Scheduling of Graph Algorithms on a Shared-Memory Platform*, International Conference for High Performance Computing, Networking, Storage, and Analysis (SC), November 2019.

24. Bhargava Gopireddy and Josep Torrellas, *Designing Vertical Processors in Monolithic 3D*, International Symposium on Computer Architecture (ISCA), June 2019. **Selected as an Honorable Mention in IEEE Micro 2020 Top Picks from Computer Architecture Conferences.**

25. Mengjia Yan, Jen-Yang Wen, Christopher Fletcher, and Josep Torrellas, *SecDir: A Secure Directory to Defeat Directory Side-Channel Attacks*, International Symposium on Computer Architecture (ISCA), June 2019.

26. Dimitrios Skarlatos, Mengjia Yan, Bhargava Gopireddy, Read Sprabery, Josep Torrellas, and Christopher Fletcher, *MicroScope: Enabling Microarchitectural Replay Attacks*, International Symposium on Computer Architecture (ISCA), June 2019. **Selected as an IEEE Micro 2020 Top Pick from Computer Architecture Conferences.**

27. Thomas Shull, Jian Huang, Josep Torrellas, *AutoPersist: An Easy-To-Use Java NVM Framework Based on Reachability*, International Conference on Programming Language Design and Implementation (PLDI), June 2019.

28. Jiho Choi, Thomas Shull, and Josep Torrellas, *Reusable Inline Caching for JavaScript Performance*, International Conference on Programming Language Design and Implementation (PLDI), June 2019.

29. Vimuth Fernando, Antonio Franques, Sergi Abadal, Sasa Misailovic, and Josep Torrellas, *Replica: A Wireless Manycore for Communication-Intensive and Approximate Data*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April 2019.

30. Sergi Abadal, Adrian Marruedo, Antonio Franques, Hamidreza Taghvaee, Albert Cabellos-Aparicio, Jin Zhou, Josep Torrellas, and Eduard Alarcon, *Opportunistic Beamforming in Wireless Network-on-Chip*, International Symposium on Circuits and Systems (ISCAS), May 2019.

31. Thomas Shull, Jian Huang, and Josep Torrellas, *QuickCheck: Using Speculation to Reduce the Overhead of Checks in NVM Frameworks*, International Conference on Virtual Execution Environments (VEE), April 2019.

32. Thomas Shull, Jiho Choi, Maria J. Garzaran, and Josep Torrellas, *NoMap: Speeding-Up JavaScript Using Hardware Transactional Memory*, International Symposium on High-Performance Computer Architecture (HPCA), February 2019.

33. Apostolos Kokolis, Dimitrios Skarlatos, and Josep Torrellas, *PageSeer: Using Page Walks to Trigger Page Swaps in Hybrid Memory Systems*, International Symposium on High-Performance Computer Architecture (HPCA), February 2019.

34. Mengjia Yan, Read Sprabery, Bhargava Gopireddy, Christopher Fletcher, Roy Campbell, and Josep Torrellas, *Attack Directories, Not Caches: Side Channel Attacks in a Non-Inclusive World*, IEEE Symposium on Security and Privacy (SP), May 2019.

35. Mengjia Yan, Jiho Choi, Dimitrios Skarlatos, Adam Morrison, Christopher W. Fletcher, and Josep Torrellas, *InvisiSpec: Making Speculative Execution Invisible in the Cache Hierarchy*, International Symposium on Microarchitecture (MICRO), October 2018. **Honorable Mention in 2019 IEEE Micro's Top Picks from Computer Architecture Conferences**.

36. Raghavendra Pradyumna Pothukuchi, Sweta Yamini Pothukuchi, Josep Torrellas, and Petros Voulgaris, *Modular Computer Resource Management with Multiple Structured Singular Value Controllers*, IEEE Conference on Decision and Control (CDC), December 2018.

37. Jiho Choi, Thomas Shull, and Josep Torrellas, *Biased Reference Counting: Limiting Atomic Operations in Reference Counting for Garbage Collection*, International Conference on Parallel Architectures and Compilation Techniques (PACT), November 2018.

38. Zhangxiaowen Gong, Zhi Chen, Justin Szaday, David Wong, Zehra Sura, Neftali Watkinson, Saeed Maleki, David Padua, Alexander Veidenbaum, Alexandru Nicolau, and Josep Torrellas, *An Empirical Study of the Effect of Source-level Loop Transformations on Compiler Stability*, Conference on Object-Oriented Programming, Systems, Languages and Applications (OOPSLA), November 2018.

39. Thomas Shull, Jian Huang, and Josep Torrellas, *Defining a High-Level Programming Model for Emerging NVRAM Technologies*, International Conference on Managed Languages and Runtimes (ManLang), September 2018.

40. Bhargava Gopireddy, Dimitrios Skarlatos, Wenjuan Zhu, and Josep Torrellas, *HetCore: TFET-CMOS Hetero-Device Architecture for CPUs and GPUs*, International Symposium on Computer Architecture (ISCA), June 2018.

41. Raghavendra Pradyumna Pothukuchi, Sweta Yamini Pothukuchi, Petros Voulgaris, and Josep Torrellas, *Yukta: Multilayer Resource Controllers to Maximize Efficiency*, International Symposium on Computer Architecture (ISCA), June 2018.

42. Xavier Timoneda, Sergi Abadal, Albert Cabellos-Aparicio, Dionysios Manessis, Jin Zhou, Antonio Franques, Josep Torrellas and Eduard Alarcon, *Millimeter-Wave Propagation Within a Computer Chip Package*, International Symposium on Circuits and Systems (ISCAS), May 2018.

43. Yasser Shalabi, Mengjia Yan, Nima Honarmand, Ruby Lee, and Josep Torrellas, *RnR-Safe: Record-Replay Architecture as a General Security Framework*, International Symposium on High-Performance Computer Architecture (HPCA), February 2018.

44. Dimitrios Skarlatos, Nam Sung Kim, and Josep Torrellas, *PageForge: A Near-Memory Content-Aware Page-Merging Architecture*, International Symposium on Microarchitecture (MICRO), October 2017.

45. Aditya Agrawal, Josep Torrellas, and Sachin Idgunji, *Xylem: Enhancing Vertical Thermal Conduction in 3D Processor-Memory Stacks*, International Symposium on Microarchitecture (MICRO), October 2017.

46. Zhi Chen, Zhangxiaowen Gong, Justin Szaday, David Wong, David Padua, Alexandru Nicolau, Alexander Veidenbaum, Neftali Watkinson, Zehra Sura, Saeed Maleki, Josep Torrellas, and Gerald DeJong, *LORE: A Loop Repository for the Evaluation of Compilers*, International Symposium on Workload Characterization (IISWC), October 2017.

47. Raghavendra Pothukuchi, Amin Ansari, Bhargava Gopireddy, and Josep Torrellas, *Sthira: A Formal Approach to Minimize Voltage Guardbands under Variation in Networks-on-Chip for Energy Efficiency*, International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2017. **Best Paper Nominee.**

48. Jiho Choi, Thomas Shull, Maria Garzaran, and Josep Torrellas, *ShortCut: Architectural Support for Fast Object Access in Scripting Languages*, International Symposium on Computer Architecture (ISCA), June 2017.

49. Mengjia Yan, Bhargava Gopireddy, Thomas Shull, and Josep Torrellas, *Secure Hierarchy-Aware Cache Replacement Policy (SHARP): Defending Against Cache-Based Side Channel Attacks*, International Symposium on Computer Architecture (ISCA), June 2017.

50. Sanket Tavarageri, Wooil Kim, Josep Torrellas, and P. Sadayappan, *Compiler Support for Software Cache Coherence*, International Conference on High Performance Computing, Data, and Analytics (HiPC), December 2016.

51. Mengjia Yan, Yasser Shalabi, and Josep Torrellas, *ReplayConfusion: Detecting Cache-based Covert Channel Attacks Using Record and Replay*, International Symposium on Microarchitecture (MICRO), October 2016.

52. Dimitrios Skarlatos, Renji Thomas, Aditya Agrawal, Shibin Qin, Robert Pilawa, Ulya Karpuzcu, Radu Teodorescu, Nam Sung Kim, and Josep Torrellas, *Snatch: Opportunistically Reassigning Power Allocation between Processor and Memory in 3D Stacks*, International Symposium on Microarchitecture (MICRO), October 2016.

53. Sanyam Mehta and Josep Torrellas, *WearCore: A Core for Wearable Workloads*, International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2016.

54. Raghavendra Pothukuchi, Amin Ansari, Petros Voulgaris, and Josep Torrellas, *Using Multiple Input, Multiple Output Formal Control to Maximize Resource Efficiency in Architectures*, International Symposium on Computer Architecture (ISCA), June 2016.

55. Wooil Kim, Sanket Tavarageri, Ponnuswamy Sadayappan, and Josep Torrellas, *Architecting and Programming a Hardware-Incoherent Multiprocessor Cache Hierarchy*, International Parallel and Distributed Processing Symposium (IPDPS), May 2016.

56. Tanmay Gangwani, Adam Morrison, and Josep Torrellas, *CASPAR: Breaking Serialization in Lock-Free Multicore Synchronization*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April 2016.

57. Sergi Abadal, Albert Cabellos-Aparicio, Eduard Alarcon and Josep Torrellas, *WiSync: An Architecture for Fast Synchronization through On-Chip Wireless Communication*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), April 2016.

58. Yuelu Duan, David Koufaty, and Josep Torrellas, *SCsafe: Logging Sequential Consistency Violations Continuously and Precisely*, International Symposium on High Performance Computer Architecture (HPCA), March 2016.

59. Bhargava Gopireddy, Choungki Song, Josep Torrellas, Nam Sung Kim, Aditya Agrawal, and Asit Mishra, *ScalCore: Designing a Core for Voltage Scalability*, International Symposium on High Performance Computer Architecture (HPCA), March 2016.

60. Yuelu Duan, Nima Honarmand and Josep Torrellas, *Asymmetric Memory Fences: Optimizing Both Performance and Implementability*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2015.

61. Ehsan Totoni, Josep Torrellas, and Laxmikant V. Kale, *Using an Adaptive HPC Runtime System to Reconfigure the Cache Hierarchy*, International Conference for High Performance Computing, Networking, Storage and Analysis (SC), November 2014.

62. Nima Honarmand and Josep Torrellas, *Replay Debugging: Leveraging Record and Replay for Program Debugging*, International Symposium on Computer Architecture (ISCA), June 2014.

63. Xuehai Qian, Benjamin Sahelices, and Josep Torrellas, *OmniOrder: Directory-Based Coherence for Conflict Serialization*, International Symposium on Computer Architecture (ISCA), June 2014.

64. Wonsun Ahn, Jiho Choi, Thomas Shull, Maria Garzaran, and Josep Torrellas, *Improving JavaScript Performance Through Predictable Type Specialization* International Conference on Programming Language Design and Implementation (PLDI), June 2014. **Distinguished Paper Award**.

65. Nima Honarmand and Josep Torrellas, *RelaxReplay: Record and Replay for Relaxed-Consistency Multiprocessors*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2014.

66. Josep Torrellas, *Extreme-Scale Computer Architecture: Energy Efficiency from the Ground Up*, Design Automation and Test in Europe (DATE), March 2014.

67. Aditya Agrawal, Amin Ansari, and Josep Torrellas, *Mosaic: Exploiting the Spatial Locality of Process Variation to Reduce Refresh Energy in On-Chip eDRAM Modules*, International Symposium on High Performance Computer Architecture (HPCA), February 2014.

68. Amin Ansari, Asit Mishra, Jianping Xu, and Josep Torrellas, *Tangle: Route-Oriented Dynamic Voltage Minimization for Variation-Afflicted, Energy-Efficient On-Chip Networks*, International Symposium on High Performance Computer Architecture (HPCA), February 2014.

69. Shanxiang Qi, Abdullah Muzahid, Wonsun Ahn, and Josep Torrellas, *Dynamically Detecting and Tolerating IF-Condition Data Races*, International Symposium on High Performance Computer Architecture (HPCA), February 2014.

70. Xuehai Qian, Benjamin Sahelices, Josep Torrellas, and Depei Qian, *BulkCommit: Scalable and Fast Commit of Atomic Blocks in a Lazy Multiprocessor Environment*, International Symposium on Microarchitecture (MICRO), December 2013.

71. Gilles Pokam, Klaus Danne, Cristiano Pereira, Rolf Kassa, Tim Kranich, Shiliang Hu, and Justin Gottschlich (Intel), and Nima Honarmand, Nathan Dautenhahn, Sam King and Josep Torrellas (UIUC), *QuickRec: Prototyping an Intel Architecture Extension for Record and Replay of Multithreaded Programs*, International Symposium on Computer Architecture (ISCA), June 2013.

72. Yuelu Duan, Abdullah Muzahid, and Josep Torrellas, *WeeFence: Toward Making Fences Free in TSO*, International Symposium on Computer Architecture (ISCA), June 2013.

73. Wonsun Ahn, Yuelu Duan and Josep Torrellas, *DeAliaser: Alias Speculation Using Atomic Region Support*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2013.

74. by Nima Honarmand, Nathan Dautenhahn, Josep Torrellas, Samuel King, Gilles Pokam and Cristiano Pereira, *Cyrus: Unintrusive Application-Level Record-Replay for Replay Parallelism*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2013.

75. Xuehai Qian, Benjamin Sahelices, Josep Torrellas and Depei Qian, *Volition: Scalable and Precise Sequential Consistency Violation Detection*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2013.

76. Nicholas P. Carter, Aditya Agrawal, Shekhar Borkar, Romain Cledat, Howard David, Dave Dunning, Joshua Fryman, Ivan Ganev, Roger A. Golliver, Rob Knauerhase, Richard Lethin, Benoit Meister, Asit K. Mishra, Wilfred R. Pinfold, Justin Teller, Josep Torrellas, Nicolas Vasilache, Ganesh Venkatesh, and Jianping Xu, *Runnemede: An Architecture for Ubiquitous High-Performance Computing*, International Symposium on High Performance Computer Architecture (HPCA), February 2013.

77. Ulya R. Karpuzcu, Abhishek Sinkar, Nam Sung Kim, and Josep Torrellas, *EnergySmart: Toward Energy-Efficient Manycores for Near-Threshold Computing*, International Symposium on High Performance Computer Architecture (HPCA), February 2013.

78. Aditya Agrawal, Prabhat Jain, Amin Ansari and Josep Torrellas, *Refrint: Intelligent Refresh to Minimize Power in On-Chip Multiprocessor Cache Hierarchies*, International Symposium on High Performance Computer Architecture (HPCA), February 2013.

79. Amin Ansari, Shuguang Feng, Shantanu Gupta, Josep Torrellas, and Scott Mahlke, *Illusionist: Transforming Lightweight Cores into Aggressive Cores on Demand*, International Symposium on High Performance Computer Architecture (HPCA), February 2013.

80. Abdullah Muzahid, Shanxiang Qi and Josep Torrellas, *Vulcan: Hardware Support for Detecting Sequential Consistency Violations Dynamically*, International Symposium on Microarchitecture (MICRO), December 2012.

81. Josep Torrellas, *FlexRAM: Toward an Advanced Intelligent Memory System. A Retrospective Paper*, International Conference on Computer Design (ICCD), September 2012.

82. Ulya R. Karpuzcu, Krishna B. Kolluru, Nam Sung Kim and Josep Torrellas, *VARIUS-NTV: A Microarchitectural Model to Capture the Increased Sensitivity of Manycores to Process Variations at Near-Threshold Voltages*, International Conference on Dependable Systems and Networks (DSN), June 2012. Acceptance Rate: 17%.

83. Ehsan Totoni, Babak Behzad, Swapnil Ghike and Josep Torrellas, *Comparing the Power and Performance of Intel's SCC to State-of-the-Art CPUs and GPUs*, International Symposium on Performance Analysis of Systems and Software (ISPASS), April 2012.

84. Xuehai Qian, Benjamin Sahelices and Josep Torrellas, *BulkSMT: Designing SMT Processors for Atomic-Block Execution*, International Symposium on High Perfomance Computer Architecture (HPCA), February 2012.

85. Shanxiang Qi, Norimasa Otsuki, Lois Orosa, Abdullah Muzahid, and Josep Torrellas, *Pacman: Tolerating Asymmetric Data Races with Unintrusive Hardware*, International Symposium on High Perfomance Computer Architecture (HPCA), February 2012.

86. Yuelu Duan, Xing Zhou, Wonsun Ahn, and Josep Torrellas, *BulkCompactor: Optimized Deterministic Execution via Conflict-Aware Commit of Atomic Blocks*, International Symposium on High Perfomance Computer Architecture (HPCA), February 2012.

87. Rishi Agarwal and Josep Torrellas, *FlexBulk: Intelligently Forming Atomic Blocks in Blocked-Execution Multiprocessors to Minimize Squashes*, International Symposium on Computer Architecture (ISCA), June 2011.

88. Rishi Agarwal, Pranav Garg, and Josep Torrellas, *Rebound: Scalable Checkpointing for Coherent Shared Memory*, International Symposium on Computer Architecture (ISCA), June 2011.

89. Xuehai Qian, Wonsun Ahn, and Josep Torrellas, *ScalableBulk: Scalable Cache Coherence for Atomic Blocks in a Lazy Environment*, International Symposium on Microarchitecture (MICRO), December 2010. (17% acceptance rate).

90. Abdullah Muzahid, Norimasa Otsuki, and Josep Torrellas, *AtomTracker: A Comprehensive Approach to Atomic Region Inference and Violation Detection*, International Symposium on Microarchitecture (MICRO), December 2010. (17% acceptance rate).

91. Adrian Nistor, Darko Marinov, and Josep Torrellas, *InstantCheck: Checking the Determinism of Parallel Programs Using On-the-fly Incremental Hashing*, International Symposium on Microarchitecture (MICRO), December 2010. (17% acceptance rate).

92. Brian Greskamp, Ulya R. Karpuzcu, and Josep Torrellas, *LeadOut: Composing Low-Overhead Frequency-Enhancing Techniques for Single-Thread Performance in Configurable Multicores*, International Symposium on High-Performance Computer Architecture (HPCA), January 2010.

93. Wonsun Ahn, Shanxiang Qi, Jae-Woo Lee, Marios Nicolaides, Xing Fang, Josep Torrellas, David Wong, and Samuel Midkiff, *BulkCompiler: High-Performance Sequential Consistency through Cooperative Compiler and Hardware Support*, International Symposium on Microarchitecture (MICRO), December 2009.

94. Ulya R. Karpuzcu, Brian Greskamp and Josep Torrellas, *The BubbleWrap Many-Core: Popping Cores for Sequential Acceleration*, International Symposium on Microarchitecture (MICRO), December 2009. **Best Paper Award**.

95. Adrian Nistor, Darko Marinov, and Josep Torrellas, *Light64: Lightweight Hardware Support for Race Detection during Systematic Testing of Parallel Programs*, International Symposium on Microarchitecture (MICRO), December 2009.

96. Abdullah Muzahid, Dario Suarez, Shanxiang Qi, and Josep Torrellas, *SigRace: Signature-Based Data Race Detection*, International Symposium on Computer Architecture (ISCA), June 2009.

97. Pablo Montesinos, Matthew Hicks, Samuel T. King, and Josep Torrellas, *Capo: A Software-Hardware Interface for Practical Deterministic Multiprocessor Replay*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2009.

98. Brian Greskamp, R. Ulya Karpuzcu, and Josep Torrellas, *BubbleWrap: Popping CMP Cores for Sequential Acceleration*, Wild and Crazy Ideas Session, at International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2009. **Best Idea Award**.

99. Brian Greskamp, Lu Wan, Ulya R. Karpuzcu, Jeffrey J. Cook, Josep Torrellas, Deming Chen, and Craig Zilles, *BlueShift: Designing Processors for Timing Speculation from the Ground Up*, International Symposium on High-Performance Computer Architecture (HPCA), February 2009.

100. Abhishek Tiwari and Josep Torrellas, *Facelift: Hiding and Slowing Down Aging in Multicores*, International Symposium on Microarchitecture (MICRO), November 2008.

101. Smruti Sarangi, Brian Greskamp, Abhishek Tiwari, and Josep Torrellas, *EVAL: Utilizing Processors with Variation-Induced Timing Errors*, International Symposium on Microarchitecture (MICRO), November 2008.

102. Pablo Montesinos, Luis Ceze, and Josep Torrellas, *DeLorean: Recording and Deterministically Replaying Shared-Memory Multiprocessor Execution Efficiently*, International Symposium on Computer Architecture (ISCA), June 2008.

103. Radu Teodorescu and Josep Torrellas, *Variation-Aware Application Scheduling and Power Management for Chip Multiprocessors*, International Symposium on Computer Architecture (ISCA), June 2008.

104. James Tuck, Wonsun Ahn, Luis Ceze, and Josep Torrellas, *SoftSig: Software-Exposed Hardware Signatures for Code Analysis and Optimization*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), March 2008.

105. Karin Strauss, Xiaowei Shen, and Josep Torrellas, *Unconstrained Snoop Request Delivery in Embedded-Ring Multiprocessors*, International Symposium on Microarchitecture (MICRO), December 2007.

106. Radu Teodorescu, Jun Nakano, Abhishek Tiwari and Josep Torrellas, *Mitigating Parameter Variation with Dynamic Fine-Grain Body Biasing*, International Symposium on Microarchitecture (MICRO), December 2007.

107. James Tuck, Wei Liu, and Josep Torrellas, *CAP: Criticality Analysis for Power-Efficient Speculative Multithreading*, International Conference on Computer Design (ICCD), October 2007.

108. Cyrus Bazeghi, Francisco J. Mesa-Martinez, Brian Greskamp, Josep Torrellas, and Jose Renau, *Estimating Design Time for System Circuits*, International Conference on Very Large Scale Integration (VLSI-SoC), October 2007.

109. Brian Greskamp and Josep Torrellas, *Paceline: Improving Single-Thread Performance in Nanoscale CMPs through Core Overclocking*, International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2007.

110. Luis Ceze, James M. Tuck, Pablo Montesinos, and Josep Torrellas, *BulkSC: Bulk Enforcement of Sequential Consistency*, International Symposium on Computer Architecture (ISCA), June 2007.

111. Abhishek Tiwari, Smruti Sarangi, and Josep Torrellas, *ReCycle: Pipeline Adaptation to Tolerate Parameter Variation*, International Symposium on Computer Architecture (ISCA), June 2007.

112. Pablo Montesinos, Wei Liu, and Josep Torrellas, *Using Register Lifetime Predictions to Protect Register Files Against Soft Errors*, International Conference on Dependable Systems and Networks (DSN), June 2007.

113. Brian Greskamp, Smruti Sarangi, and Josep Torrellas, *Threshold Voltage Variation Effects on Aging-Related Hard Failure Rates*, International Symposium on Circuits and Systems (ISCAS), Special Session: Circuit Design in the Presence of Device Variability, May 2007.

114. Smruti Sarangi, Brian Greskamp, and Josep Torrellas, *A Model for Timing Errors in Processors with Parameter Variation*, International Symposium on Quality Electronic Design (ISQED), March 2007.

115. Luis Ceze, Pablo Montesinos, Christoph von Praun, and Josep Torrellas, *Colorama: Architectural Support for Data-Centric Synchronization*, International Symposium on High-Performance Computer Architecture (HPCA), February 2007.

116. Smruti R. Sarangi, Abhishek Tiwari, and Josep Torrellas, *Phoenix: Detecting and Recovering from Permanent Processor Design Bugs with Programmable Hardware*, International Symposium on Microarchitecture (MICRO), December 2006. **Best Paper Award.**

117. James Tuck, Luis Ceze, and Josep Torrellas, *Scalable Cache Miss Handling for High Memory-Level Parallelism*, International Symposium on Microarchitecture (MICRO), December 2006.

118. Shan Lu, Pin Zhou, Wei Liu, Yuanyuan Zhou, and Josep Torrellas, *PathExpander: Architectural Support for Increasing the Path Coverage of Dynamic Bug Detection*, International Symposium on Microarchitecture (MICRO), December 2006.

119. Pablo Montesinos, Wei Liu, and Josep Torrellas, *Shield: Cost-Effective Soft-Error Protection for Register Files*, Third IBM TJ Watson Conference on Interaction between Architecture, Circuits and Compilers (P=AC2), October 2006.

120. L. Ceze, J. Tuck, C. Cascaval, and J. Torrellas, *Bulk Disambiguation of Speculative Threads in Multiprocessors*, International Symposium on Computer Architecture (ISCA), June 2006.

121. K. Strauss, X. Shen, and J. Torrellas, *Flexible Snooping: Adaptive Forwarding and Filtering of Snoops in Embedded-Ring Multiprocessors*, International Symposium on Computer Architecture (ISCA), June 2006.

122. S. Sarangi, B. Greskamp, and J. Torrellas, *CADRE: Cycle-Accurate Deterministic Replay for Hardware Debugging*, International Conference on Dependable Systems and Networks (DSN), June 2006.

123. W. Liu, J. Tuck, L. Ceze, W. Ahn, K. Strauss, J. Renau and J. Torrellas, *POSH: A TLS Compiler that Exploits Program Structure*, Symposium on Principles and Practice of Parallel Programming (PPoPP), March 2006.

124. J. Nakano, P. Montesinos, K. Gharachorloo, and J. Torrellas, *ReViveI/O: Efficient Handling of I/O in Highly-Available Rollback-Recovery Servers*, International Symposium on High-Performance Computer Architecture (HPCA), February 2006.

125. S. Sarangi, W. Liu, J. Torrellas, and Y. Zhou, *ReSlice: Selective Re-Execution of Long-Retired Misspeculated Instructions Using Forward Slicing*, International Symposium on Microarchitecture (MICRO), November 2005.

126. W. Liu, J. Tuck, L. Ceze, K. Strauss, J. Renau, and J. Torrellas, *POSH: A Profiler-Enhanced TLS Compiler that Leverages Program Structure*, Watson Conference on Interaction between Architecture, Circuits, and Compilers (P=AC2), September 2005.

127. M. Wei, M. Snir, J. Torrellas, and R. B. Tremaine, *A Near-Memory Processor for Vector, Streaming and Bit Manipulation Workloads*, Watson Conference on Interaction between Architecture, Circuits, and Compilers (P=AC2), September 2005.

128. J. Renau, K. Strauss, L. Ceze, W. Liu, S. Sarangi, J. Tuck, and J. Torrellas, *Thread-Level Speculation on a CMP Can Be Energy Efficient*, International Conference on Supercomputing (ICS), June 2005.

129. J. Renau, J. Tuck, W. Liu, L. Ceze, K.Strauss, and J. Torrellas, *Tasking with Out-of-Order Spawn in TLS Chip Multiprocessors: Microarchitecture and Compilation*, International Conference on Supercomputing (ICS), June 2005.

130. R. Teodorescu and J. Torrellas, *Prototyping Architectural Support for Program Rollback Using FPGAs*, Symposium on Field-Programmable Custom Computing Machines (FCCM), April 2005.

131. P. Zhou, W. Liu, F. Long, S. Lu, F. Qin, Y. Zhou, S. Midkiff and J. Torrellas, *AccMon: Automatically Detecting Memory-Related Bugs via Program Counter-Based Invariants*, International Symposium on Microarchitecture (MICRO), December 2004.

132. P. Zhou, F. Qin, W. Liu, Y. Zhou, and J. Torrellas, *iWatcher: Efficient Architectural Support for Software Debugging*, International Symposium on Computer Architecture (ISCA), June 2004.

133. A. Nguyen and J. Torrellas, *Design Trade-offs in High-Throughput Coherence Controllers*, International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2003. Acceptance Rate: 17%.

134. M. Garzaran, M. Prvulovic, J. Llaberia, V. Vinals, L. Rauchwerger, and J. Torrellas, *Using Software Logging to Support Multi-Version Buffering in Thread-Level Speculation*, International Conference on Parallel Architectures and Compilation Techniques (PACT), September 2003. Acceptance Rate: 17%.

135. B. Fraguela, J. Renau, P. Feautrier, D. Padua, and Josep Torrellas, *Programming the FlexRAM Parallel Intelligent Memory System*, International Symposium on Principles and Practice of Parallel Programming (PPoPP), June 2003.

136. M. Prvulovic and J. Torrellas, *ReEnact: Using Thread-Level Speculation to Debug Data Races in Multithreaded Codes*, International Symposium on Computer Architecture (ISCA), June 2003.

137. M. Huang, J. Renau, and J. Torrellas, *Positional Adaptation of Processors: Application to Energy Reduction*, International Symposium on Computer Architecture (ISCA), June 2003.

138. M. Garzaran, M. Prvulovic, J. Llaberia, V. Vinals, L. Rauchwerger, and J. Torrellas, *Tradeoffs in Buffering Memory State for Thread-Level Speculation in Multiprocessors*, International Symposium on High-Performance Computer Architecture (HPCA), February 2003.

139. J. Martinez, J. Renau, M. Huang, M. Prvulovic, and J. Torrellas, *Cherry: Checkpointed Early Resource Recycling in Out-of-order Microprocessors*, International Symposium on Microarchitecture (MICRO), November 2002.

140. J. Martinez and J. Torrellas, *Speculative Synchronization: Applying Thread-Level Speculation to Parallel Applications*, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), October 2002. Acceptance Rate: 18%.

141. M. Huang, J. Renau, and J. Torrellas, *Energy-Efficient Hybrid Wakeup Logic*, International Symposium on Low Power Electronics and Design (ISLPED), August 2002. Acceptance Rate: 24%.

142. M. Prvulovic, Z. Zhang, and J. Torrellas. *ReVive: Cost-Effective Architectural Support for Rollback Recovery in Shared-Memory Multiprocessors*, International Symposium on Computer Architecture (ISCA), May 2002. Acceptance Rate: 15%.

143. Y. Solihin, J. Lee, and J. Torrellas, *Using a User-Level Memory Thread for Correlation Prefetching*, International Symposium on Computer Architecture (ISCA), May 2002. Acceptance Rate: 15%.

144. M. Cintra and J. Torrellas, *Eliminating Squashes Through Learning Cross-Thread Violations in Speculative Parallelization for Multiprocessors*, Eigth International Symposium on High-Performance Computer Architecture (HPCA), February 2002.

145. M. Garzaran, M. Prvulovic, A. Jula, H. Yu, Y. Zhang, L. Rauchwerger, and J. Torrellas, *Architectural Support for Parallel Reductions in Scalable Shared-Memory Multiprocessors*, International Conference on Parallel Architectures and Compilation Techniques (PACT), Barcelona, September 2001.

146. M. Huang, J. Renau, S.-M. Yoo, and J. Torrellas, *L1 Data Cache Decomposition for Energy Efficiency*, International Symposium on Low Power Electronics and Design (ISLPED), pp. 10-15, August 2001. Acceptance Rate: 24%.

147. M. Prvulovic, M. J. Garzaran, L. Rauchwerger, and J. Torrellas. *Removing Architectural Bottlenecks to the Scalability of Speculative Parallelization*, International Symposium on Computer Architecture (ISCA), pp. 204-215, June 2001. Acceptance Rate: 14%.

148. J. Lee, Y. Solihin, and J. Torrellas, *Automatically Mapping Code on an Intelligent Memory Architecture*, International Symposium on High-Performance Computer Architecture (HPCA), pp 121-132, January 2001. Acceptance Rate: 23%.

149. M. Huang, J. Renau, S.-M. Yoo, and J. Torrellas, *A Framework for Dynamic Energy Efficiency and Temperature Management*, International Symposium on Microarchitecture (MICRO), pp 202-213, December 2000. Acceptance Rate: 28%.

150. Q. Cao, J. Torrellas, and H.-V. Jagadish, *Unified Fine-Granularity Buffering of Index and Data: Approach and Implementation*, International Conference on Computer Design (ICCD), September 2000.

151. M. Cintra, J. Martinez and J. Torrellas, *Architectural Support for Scalable Speculative Parallelization in Shared-Memory Multiprocessors*, International Symposium on Computer Architecture (ISCA), pp 13-24, June 2000. Acceptance Rate: 17%.

152. J. Torrellas, L. Yang and A. Nguyen, *Toward a Cost-Effective DSM Organization that Exploits Processor-Memory Integration*, International Symposium on High-Performance Computer Architecture (HPCA), pp. 15-25, January 2000. Acceptance Rate: 21%.

153. Y. Kang, M. Huang, S.-M. Yoo, Z. Ge, D. Keen, V. Lam, P. Pattnaik and J. Torrellas. *FlexRAM: An Advanced Intelligent Memory System*, International Conference on Computer Design (ICCD), 192-201, October 1999. Acceptance Rate: 32%.

154. Q. Cao, P. Trancoso, J.-L. Larriba-Pey, J. Torrellas, R. Knighten and Y. Won. *Detailed Characterization of a Quad Pentium Pro Server Running TPC-D*, International Conference on Computer Design (ICCD), pp 108-115, October 1999. Acceptance Rate: 32%.

155. P. Trancoso and J. Torrellas. *Cache Optimization for Memory-Resident Decision Support Commercial Workloads*, International Conference on Computer Design (ICCD), pp 546-554, October 1999. Acceptance Rate: 32%.

156. Y. Solihin, V. Lam, and J. Torrellas, *Scal-Tool: Pinpointing and Quantifying Scalability Bottlenecks in DSM Multiprocessors*, Supercomputing 99, November 1999.

157. V. Krishnan and J. Torrellas, *The Need for Fast Communication in Hardware-Based Speculative Chip Multiprocessors*, International Conference on Parallel Architectures and Compilation Techniques (PACT), October 1999.

158. A. Ramirez, J.-L. Larriba-Pey, C. Navarro, X. Serrano, J. Torrellas, and M. Valero. *Optimization of Instruction Fetch for Decision Support Workloads*, International Conference on Parallel Processing (ICPP), September 1999. Acceptance Rate: 32%.

159. D. Koufaty and J. Torrellas. *Compiler Support for Data Forwarding in Scalable Shared-Memory Multiprocessors*, International Conference on Parallel Processing (ICPP), September 1999. Acceptance Rate: 32%.

160. J. Martinez, J. Torrellas, and J. Duato. *Improving the Performance of Bristled CC-NUMA Systems Using Virtual Channels and Adaptivity*, International Conference on Supercomputing (ICS), June 1999.

161. A. Ramirez, J.-L. Larriba-Pey, C. Navarro, J. Torrellas, and M. Valero. *Software Trace Cache*, International Conference on Supercomputing (ICS), June 1999. Acceptance Rate: 31%.

162. Y. Zhang, L. Rauchwerger and J. Torrellas. *Hardware for Speculative Parallelization of Partially-Parallel Loops in DSM Multiprocessors*, International Symposium on High-Performance Computer Architecture (HPCA), January 1999. Acceptance Rate: 31%.

163. J.Torrellas. *Upcoming Architectural Advances in DSM Machines and Their Impact on Programmability*, SIAM Conference on Parallel Processing for Scientific Computing, March 1999.

164. V. Krishnan and J. Torrellas. *A Direct-Execution Framework for Fast and Accurate Simulation of Superscalar Processors*, in International Conference on Parallel Architectures and Compilation Techniques (PACT), October 1998.

165. Y. Kang, J. Torrellas, and T. Huang. *An IRAM Architecture for Image Analysis and Pattern Recognition*, in International Conference on Pattern Recognition, 1998.

166. V. Krishnan and J. Torrellas. *Hardware and Software Support for Speculative Execution of Sequential Binaries on a Chip-Multiprocessor*, in International Conference on Supercomputing (ICS), July 1998.

167. D. Koufaty and J. Torrellas. *Comparing Data Forwarding and Data Prefetching for Communication-Induced Misses in Shared-Memory MPs*, in International Conference on Supercomputing (ICS), July 1998.

168. V. Krishnan and J. Torrellas. *A Clustered Approach to Multithreaded Processors*, in International Parallel Processing Symposium (IPPS), March 1998.

169. Y. Zhang, L. Rauchwerger, and J. Torrellas. *Hardware for Speculative Run-Time Parallelization in Distributed Shared-Memory Multiprocessors*, International Symposium on High-Performance Computer Architecture (HPCA), February 1998. Acceptance Rate: 22%.

170. S. Basu and J. Torrellas. *Enhancing Memory Use in Simple Coma: Multiplexed Simple Coma*, International Symposium on High-Performance Computer Architecture (HPCA), February 1998. Acceptance Rate: 22%.

171. P. Trancoso, J. Larriba, Z. Zhang and J. Torrellas. *The Memory Performance of DSS Commercial Workloads in Shared-Memory Multiprocessors*, International Symposium on High-Performance Computer Architecture (HPCA), February 1997. Acceptance Rate: 20%.

172. Z. Zhang and J. Torrellas. *Reducing Remote Conflict Misses: NUMA with Remote Cache versus COMA*, International Symposium on High-Performance Computer Architecture (HPCA), February 1997. Acceptance Rate: 20%.

173. L. Yang and J. Torrellas. *Speeding up the Memory Hierarchy in Flat COMA Multiprocessors*, International Symposium on High-Performance Computer Architecture (HPCA), February 1997. Acceptance Rate: 20%.

174. J. Torrellas and D. Padua. *The Illinois Aggressive Coma Multiprocessor Project (I-ACOMA)*, Frontiers of Massively Parallel Computation Symposium, October 1996.

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60. J.Torrellas, B.Bray, K.Cuderman, S.Goldschmidt, A.Kobrin, and A.Zimmerman. *Introductory User's Guide to the Architect's Workbench Tools*, technical report CSL-TR-88-355, Stanford Univ., May 1988.

61. J.Torrellas. *Incremental Logic Simulation Using Waveforms*, Masters Thesis, Dept. of Electrical and Computer Engineering, University of Wisconsin - Madison, December 1987.

62. J.Beetem and J.Torrellas. *Incremental Logic Simulation Using Waveforms*, technical report ECE-87-5, Univ. of Wisconsin - Madison, April 1987.

Patents

1. "Exploiting Spatial Locality to Reduce Refresh Energy in On-Chip eDRAM Modules", by Aditya B. Agrawal, Amin Ansari, and Josep Torrellas, 2013.

2. "Exposing Control of Power and Clock Gating for Software", by Nicholas P. Carter, Joshua B. Fryman, Robert C. Knauerhase, Aditya B. Agrawal, and Josep Torrellas, 2012.

3. "Architecture Support System and Method for Memory Monitoring", by Yuanyuan Zhou, Josep Torrellas, and Pin Zhou, US patent number 7,711,988, May 2010.

Editorship of Journals

Jul 17 - Oct 18 Member of the Editorial Board, Communications of the ACM (CACM).
2013 - 2014 Board of Distinguished Reviewers for the ACM TACO journal.
Mar 03 - Jan 06 Associate Editor, ACM Transactions on Architecture and Code Optimization (TACO).
Dec 01 - Jan 06 Member of the Editorial Board, IEEE Computer Architecture Letters (CAL).

Recent Research Funding

Jun 21 $200 M, IBM+UIUC+State of Illinois, lead PI: D. Chen, num PIs: 15, duration: 10 years.
Title: Discovery Accelerator Institute.

Feb 21 $160 K, Intel, lead PI: J. Torrellas, num PIs: 1, duration: 2 years.
Title: Accelerating Graph Neural Networks (GNNs) on CPUs.

Oct 20 $850 K, NSF CSR, lead PI: J. Torrellas, num PIs: 2, duration: 3 years.
Title: CNS Core: Medium: Rethinking Architecture and Operating Systems for Modern Virtualization Technologies.

Oct 20 $250 K, NSF PPoSS, lead PI: J. Torrellas, num PIs: 4, duration: 3 years.
Title: A Cross-Layer Approach to Speed-up Very Large Graph Applications on Distributed Platforms.

Oct 20 $210 K, Semiconductor Research Corporation, lead PI: J. Torrellas, num PIs: 3, duration: 3 years.
Title: Thwarting Microarchitectural Replay Attacks.

Mar 20 $53 K, Google Faculty Research Award, lead PI: C. Fletcher, num PIs: 2.
Title: Techniques to Improve Software Defenses Against Spectre Attacks.

Sep 18 $1.5 M, Intel, lead PI: C. Fletcher, num PIs: 5.
Title: Intel Strategic Research Alliance (ISRA) Center: InvisiSpec: Invisible Speculation for Secure and Efficient Speculative Execution.

Aug 18 $1.2 M, NSF CSR, lead PI: J. Torrellas, num PIs: 3.
Title: Effective Control to Maximize Resource Efficiency in Large Clusters: Hardware, Runtime, and Compiler Perspectives.

Sep 17 $500 K, NSF SPX, lead PI: J. Torrellas, num PIs: 2.
Title: Training of Deep Neural Networks Using Shared-Memory Platforms.

Nov 16 $260 K, SK Hynix, lead PI: J. Torrellas, num PIs: 1.
Title: Page Management in Hybrid DRAM-NVM Memory Systems.

Aug 16 $880 K, NSF XPS, lead PI: J. Torrellas, num PIs: 3.
Title: XPS:FULL:Breaking the Scalability Wall of Shared Memory through Fast On-Chip Wireless Communic.

Aug 16 $300 K, NSF CCF, lead PI: J. Torrellas, num PIs: 1.
Title: Eager: Technologies for Ultra Energy-Efficient Multicores.

Aug 15 $500 K, NSF CCF, lead PI: J. Torrellas, num PIs: 1.
Title: Architectures for Scripting Languages.

Sep 12 $2.8 M ($1.77M received), DARPA PERFECT, lead PI: J. Torrellas, num PIs: 3.
Title: Parameter Variation at NT Voltage: The Power Efficiency versus Resilience Tradeoff.

Sep 12 $8.4 M DOE X-Stack + $3.6M cost share, lead PI: S. Borkar, num PIs: 8.
Title: Traleika Glacier X-Stack.

Sep 12 $100 K, Mr. Bruce Ge Fund, lead PI: J. Torrellas, num PIs: 1.
Title: Improving Computer Systems.

Sep 11 $2 M Intel, plus $1.6M from the University of Illinois, lead PI: J. Torrellas, num PIs: 6.
Title: Illinois-Intel Parallelism Center (I2PC).

Jul 11 $430 K, NSF CSR, lead PI: J. Torrellas, num PIs: 1.
Title: Framework for Concurrency Debugging.

Sep 10 $2.4 M, NSF CCF, lead PI: J. Torrellas, num PIs: 4.
Title: Programmable Many-Core for Extreme Scale Computing.

Jul 10 $25.8 M DARPA UHPC, plus $23.2M from Intel, lead PI: S. Borkar, num PIs: 14.
Title: Runnemede: An Architecture for Ubiquitous High Performance Computing.

Aug 10 $1.9 M, DOE ASCR, lead PI: J. Torrellas, num PIs: 4.

	Title: Thrifty: An Exascale Architecture for Energy Proportional Computing.
May 10	$70 K, NSF CSR, lead PI: S. King, num PIs: 2.
	Title: Supplemental on Deterministic Multiprocessor Replay.
Aug 09	$23 K, DARPA TCTO, lead PI: J. Torrellas, num PIs: 1.
	Title: Study on Extreme Scale Multiprocessors.
Jun 09	$168 K, NSF CPA, lead PI: J. Torrellas, num PIs: 3.
	Title: Supplemental on Addressing the Parameter Variation Challenge.
Feb 09	$90 K cash + $30 K equipment, Sun Microsystems, lead PI: J. Torrellas, num PIs: 9.
	Title: UIUC OpenSPARC Center of Excellence.
Sep 08	$350 K, NSF CSR, lead PI: S. King, num PIs: 2.
	Title: Recording and Deterministically Replaying Shared-memory Multiprocessors.
Mar 08	$120 K cash + $50 K equipment, Sun Microsystems, lead PI: J. Torrellas, num PIs: 9.
	Title: UIUC OpenSPARC Center of Excellence.
Feb 08	$6M Intel and Microsoft, plus $4.8M from the University of Illinois, lead PI: M. Snir and W. Hwu, num PIs: 15.
	Title: Universal Parallel Computing Research Center (UPCRC).
Sep 07	$890 K, NSF CSR, lead PI: J. Torrellas, num PIs: 5.
	Title: Novel Programming Models and Architectures to Simplify Parallel Programming.
Jul 07	$1,200 K, NSF CPA, lead PI: J. Torrellas, num PIs: 3.
	Title: Addressing the Parameter-Variation Challenge through Architecture, CAD, and Compilers.
Apr 07	$360 K, Semiconductor Research Corporation, lead PI: J. Torrellas, num PIs: 2.
	Title: Timing Faults Due to Parameter Variation.
Nov 04	$40 K cash + $25 K equipment, Intel, lead PI: J. Torrellas, num PIs: 1.
	Title: Speculative Multithreading.
Nov 04	$500 K, DOE Extreme Scale Computation, lead PI: J. Nieplocha, num PIs: 6.
	Title: Scalable Fault Tolerant Runtime and OS.
Sep 03	$1,000 K, NSF Medium ITR, lead PI: J. Torrellas, num PIs: 4.
	Title: Automatic Detection and Correction of Bugs.
Jul 03	$3,000 K, DARPA-IPTO/IBM/UIUC, lead PI: J. Torrellas, num PIs: 4.
	Title: IBM PERCS High-Productivity Computer System.
Apr 03	$14 K, UIUC-CNRS, lead PI: D. Padua, num PIs: 6.
	Title: Program Optimization.
Jul 02	$100 K, DARPA-IPTO/IBM, lead PI: J. Torrellas, num PIs: 3.
	Title: IBM PERCS High-Productivity Computer System.
Sep 02	$500 K, DOD, lead PI: M. Snir, num PIs: 2.
	Title: Superconducting Switch for Teraflop Architecture.
Sep 01	$1,375 K, NSF Medium ITR, lead PI: J. Torrellas, num PIs: 2.
	Title: Novel Scalable Simulation.
Aug 01	$750 K, NSF-NGS, lead PI: D. Padua, num PIs: 3.
	Title: Open MP for Networked Computing.
Aug 01	$300 K, NSF-NGS, lead PI: L. Rauchwerger, num PIs: 3.
	Title: Application Centric Computing.
Jun 01	$2,700 K, DARPA-IPTO, lead PI: J. Torrellas, num PIs: 6.
	Title: Morphable Multithreaded Memory Tiles (M3T).
Sep 00	$1,900 K, NSF-EIA, lead PI: J. Torrellas, num PIs: 3.
	Title: FlexRAM: Intelligent Memory Architecture.
Sep 00	$500 K, NSF-ITR, lead PI: J. Torrellas, num PIs: 4.
	Title: Solving the Protein Folding Problem.
Dec 00	$750 K, IBM, lead PI: D. Reed, num PIs: 4.
	Donation of a 16-node SP2 machine.
Aug 99	$10 K, NSF-CCR, lead PI: J. Torrellas, num PIs: 1.
	HPCA travel grant.
Sep 99	$300 K, NSF-NGS, lead PI: L. Rauchwerger, num PIs: 3.
	Title: Application Centric Computing.
Jun 99	$325 K, NSF-CCR, lead PI: J. Torrellas, num PIs: 1.

	Title: New Architectures to Run Commercial Workloads.
Sep 99	$15 K, IBM, lead PI: J. Torrellas, num PIs: 1. Joint study.
Feb 98	$75 K in cash and $60 K in equip, Intel, lead PI: J. Torrellas, num PIs: 1.
	Title: Evaluating Database Workloads on Multiprocessors.
Aug 97	$25 K, Commission Scientific Exchange USA-Spain, lead PI: J. Larriba, num PIs: 3.
	Title: Multiprocessor Computer Architectures and Databases.
Jun 97	$110 K, IBM, lead PI: J. Torrellas, num PIs: 1. IBM Partnership.
Jun 97	$455 K, NSF-MIPS, lead PI: J. Torrellas, num PIs: 2.
	Title: Illinois Aggressive COMA Multiprocessor.
Jun 96	$100 K, NSF-ASC, lead PI: J. Torrellas, num PIs: 2.
	Title: Illinois Aggressive COMA Multiprocessor.
Sep 95	$1,213K, DARPA-ITO, lead PI: D. Padua, num PIs: 3.
	Title: Polaris: A Parallelizing Compiler.

Invited Lectures

- "SAVE: Sparsity-Aware Vector Engine for Accelerating DNN Training and Inference on CPUs".
  – Open Innovation Day, Samsung Electronics, March 2021.

- "Building Defenses in Processors against Speculation Attacks".
  – Yale University, February 2021.

- "Elastic Cuckoo Page Tables: Rethinking Virtual Memory Translation for Parallelism".
  – ARM Research Summit 2020, September 2020.
  – Intel Corporation, July 2020.

- "Speculation Invariance (InvarSpec): Faster Safe Execution Through Program Analysis".
  – Intel Corporation, July 2020.

- "Interdisciplinary Research at a Time of Pervasive Changes".
  – Keynote at International Symposium on High-Performance Computer Architecture (HPCA), International Conference on Principles and Practice of Parallel Programming (PPoPP), and International Symposium on Code Generation and Optimization (CGO), Febrary 2020.

- "SecDir: A Secure Directory to Defeat Directory Side-Channel Attacks".
  – Intel Corporation, April 2019.

- "Computer Architecture Beyond Performance: Security and Programmability".
  – University of California, Riverside, CA, October 2019.
  – University of Virginia, Charlottesville, VA, February 2019.

- "Extreme Energy-Efficient Computer Architectures".
  – Waseda University, Tokyo, Japan, October 2018.

- "Architectural Support for Novel Computing Paradigms".
  – Huawei, Santa Clara, CA, August 2018.

- "Toward Extreme-Scale Manycore Architectures".
  – Distinguished Speaker, Northeastern University, Boston, MA, February 2018.
  – Keynote, at International Conference on High Performance Computing, Data, and Analytics (HiPC), Hyderabad, India, December 2016.
  – At University of Southern California, Los Angeles, CA, October 2016.
  – At University of Texas, Austin, TX, September 2016.
  – At SUNY Binghamton, Binghamton, NY, September 2016.
  – At Seoul National University, Korea, June 2016.
  – Keynote, at Intern. Symp. on Performance Analysis of Systems and Software (ISPASS), April 2016.
  – Keynote, at Workshop on Big Data Benchmarks, Performance Optimization, and Emerging Hardware (BPOE), April 2016.

- ”WiSync: An Architecture for Fast Synchronization through On-Chip Wireless Communication”.
  – At ARM Research Summit, September 2016.
  – At Intel, Extreme Scale Tech. Rev. Mtg, September 2016.

- ”CASPAR: Breaking Serialization in Lock-Free Multicore Synchronization”.
  – At At Intel, Extreme Scale Tech. Rev. Mtg, May 2016.

- ”ScalCore: Designing a Core for Voltage Scalability”.
  – At Intel, Extreme Scale Technical Review Mtg, March 2016.

- ”Improving JavaScript Performance”.
  – At Intel Laboratories, Santa Clara, CA, April 2014.

- ”Toward Programmable High-Performance Multicores”.
  – At University of Washington, Seattle, WA, January 2015.
  – At Stanford University, Stanford, CA, May 2014.
  – At Qualcomm Research, San Jose, CA, December 2013.
  – At University of Cyprus, Nicosia, Cyprus, July 2013.
  – At Technion, Haifa, Israel, June 2013.
  – At Intel Haifa, Israel, June 2013.
  – At Princeton University, April 2013.
  – At Harvard University, April 2013.
  – At Massachussets Institute of Technology, April 2013.
  – At University of California Berkeley, April 2013.
  – At Intel Laboratories, Santa Clara, CA, April 2013.
  – At Carnegie-Mellon University, April 2013.

- ”Boosting the Energy Efficiency of Low-Voltage Multicores”.
  – At Qualcomm, San Diego, CA, August 2014.
  – At Qualcomm, Raleigh, NC, February 2014.
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, January 2014.
  – At AMD, Austin, TX, December 2013.
  – At Intel, Hillsboro, OR, December 2013.

- ”Tackling Parameter Variation from an Architectural Perspective”.
  – Keynote, at International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), Amsterdam, October 2014.

- ”Extreme Scale Computer Architecture: Energy Efficiency from the Ground Up”.
  – Keynote, at Workshop on Architectures and Systems for Big Data (ASBD), June 2014.
  – At Office of Technology Management, University of Illinois, October 2013.
  – Keynote, IEEE International Conference on Application-Specific Systems, Architectures and Processors (ASAP), George Washington University Virginia Science and Technology Campus, VA, June 2013.
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, February 2013.
  – Invited Speaker, Workshop on Highly-Reliable Power-Efficient Embedded Designs (HARSH), Shenzhen, China, February 2013.
  – At Shanghai Jiao Tong University, Shanghai, February 2013.
  – At National University of Defense Technology (NUDT), Changsha, China, February 2013.
  – At Institute for Computing Technology, Chinese Academy of Sciences, Beijing, December 2012.
  – At Beihang University, Beijing, December 2012.
  – At Tsinghua University, Beijing, December 2012.
  – At Pekin University, Beijing, December 2012.
  – Keynote, Workshop on Near-Threshold Computing (NTC), Vancouver, Canada, December 2012.
  – Jon Postel Distinguished Lecture, Computer Science Department, UCLA, November 2012.

- ”Vulcan: Hardware Support for Detecting Sequential Consistency Violations in Programs Dynamically”.
  – At I2PC Distinguished Speaker Series, University of Illinois, September 2012.

- ”Low Power Architectural Trends”.
  – At Nortwestern University, October 2011.

- ”Novel Techniques to Debug Multithreaded Programs”.
  – At Microsoft Research Asia, Beijing, December 2012.
  – At Intel Programming Systems Laboratory, Santa Clara, CA, October 2010.

- ”The Bulk Multicore Architecture for Programmability”.
  – At Seoul National University, Seoul, Korea, September 2011.
  – At Samsung, Seoul, Korea, September 2011.
  – At KAIST, Daejeon, Korea, September 2011.
  – At Samsung System LSI division, Seoul, Korea, September 2011.
  – At Pohang University of Science and Technology, Pohang, Korea, September 2011.
  – At University of Florida, Gainesville, FL, February 2011.
  – At University of Michigan, Ann Arbor, MI, April 2010.
  – Keynote, at 4th Workshop on Chip Multiprocessor Memory Systems and Interconnects, Bangalore, India, January 2010.
  – At Intel, Bangalore, India, January 2010.
  – At DARPA-IPTO, Washington, DC, October 2008.
  – At Stanford University, Stanford, CA, October 2008.
  – At Intel Laboratories, Hillsboro, OR, October 2008.
  – At Sun Microsystems, Santa Clara, CA, October 2008.
  – At UIUC-UPCRC Research Seminar, Urbana, IL, October 2008.
  – At Microsoft Research, Redmond, WA, September 2008.
  – At Intel Laboratories, Santa Clara, CA, August 2008.
  – At Institute for Computing Technology, Chinese Academy of Sciences, Beijing, June 2008.
  – At Tsinghua University, Beijing, June 2008.
  – At Beijing University of Aeronautics and Astronautics, Beijing, June 2008.
  – At Microsoft Research, Beijing, June 2008.
  – At IBM Research, Beijing, June 2008.
  – At Intel Laboratories, Barcelona, June 2008.
  – At Carnegie Mellon University, June 2008.
  – At University of California Berkeley, May 2008.
  – At Massachussets Institute of Technology, May 2008.
  – At Harvard University, May 2008.
  – At IBM T.J. Watson Research Center, Yorktown, NY, May 2008.
  – At Texas A&M University, April 2008.
  – At Georgia Institute of Technology, April 2008.
  – At University of Texas at Austin, April 2008.
  – At University of Tokyo, April 2008.
  – At Rice University, April 2008.

- ”Parameter Variation-Tolerant Computer Architectures”.
  – Distinguished Speaker Colloquium, ECE Department, North Carolina State University, Raleigh, NC, March 2012.
  – At IBM Research, Austin, TX, February 2011.
  – At University of Minnesota, Minneapolis, MN, December 2010.
  – At Intel, Marlborough, MA, January 2009.
  – Keynote, at Los Alamos Computer Science Symposium (LACSS), Santa Fe, October 2008.
  – At Department of Computer Science Distinguished Lectures, UIUC, Urbana, IL, October 2008.
  – Keynote, at Workshop on Quality-Aware Design, June 2008.
  – At Intel Microarchitecture Research Laboratory, Hillsboro, OR, March 2008.
  – Invited Talk at IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips X), Yokohama, Japan, April 2007.
  – At Waseda University, Tokyo, April 2007.

– Invited Talk at Third IBM TJ Watson Conference on Interaction between Architecture, Circuits and Compilers (PAC2), October 2006.
– At Department of Electrical and Computer Engineering, University of Toronto, December 2005.
– At VLSI Circuits Seminar, Department of Electrical and Computer Engineering, UIUC, October 2005.

- ”An Agenda for Parallel Computer Architecture and Parallel Computing”.
  – At Texas A&M University, April 2009.

- ”Practical Deterministic Multiprocessor Replay”.
  – At Intel Laboratories, Santa Clara, CA, December 2009.
  – At Microsoft, Redmond, WA, April 2009.
  – At Intel, Hillsboro, OR, April 2009.

- ”Designing Multicores for Single-Thread Performance”.
  – At IBM T.J. Watson Research Center, Yorktown, NY, February 2009.
  – At Sun Microsystems, Santa Clara, CA, December 2008.

- ”Speculative Multithreading Architectures”.
  – At Intel Microarchitecture Research Laboratory, Hillsboro, OR, August 2006.

- ”A Near-Memory Processor for Vector, Streaming and Bit Manipulation Workloads”.
  – At IBM PERCS Virtual Seminar, January 2005.

- ”Hardware-Supported Data Race Detection”.
  – At Intel, Champaign, IL, April 2005.
  – At Intel, Champaign, IL, November 2004.

- ”Using Thread Level Speculation for Performance and to Enhance Software Debugging and Programmability”.
  – At Cornell University, Ithaca, NY, November 2004.
  – At SUN Microsystems, Sunnyvale, CA, August 2004.
  – At Intel, Champaign IL, January 2004.
  – At Universidad Complutense de Madrid, Spain, June 2003.
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, April 2003.
  – At Intel Microprocessor Research Laboratory, Santa Clara CA, March 2003.

- ”Challenging Issues in Speculative Multithreading”.
  – At Carnegie-Mellon University, Pittsburgh PA, December 2002.
  – At University of Rochester, Rochester NY, December 2002.
  – At Intel, Marlborough, MA, May 2002.
  – At Compaq Computer, Shrewsbury, MA, May 2002.
  – At Universitat Politecnica de Catalunya, Barcelona, Spain, July 2000.

- ”FlexRAM: Toward an Advanced Intelligent Memory System”.
  – At Los Alamos National Laboratory, Los Alamos NM, September 2002.
  – At Purdue University, West Lafayette, IN, April 2002.
  – At Intel, Champaign IL, December 2001.
  – Keynote Speech at XII Jornadas Nacionales de Paralelismo, Valencia, Spain, September 2001.
  – At Los Alamos National Laboratory, Los Alamos NM, March 2001.
  – At Massachusetts Institute of Technology (MIT), February 2001.
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, October 2000.
  – At Universidad Politecnica de Madrid, Spain, January 2000.
  – At Chalmers University, Gothenburg, Sweden, December 1999.
  – At Intel Corporation, Hillsboro, OR, November 1999.
  – At Universitat Politecnica de Catalunya, Barcelona, Spain, August 1999.
  – At Univeriste de Versailles, France, July 1999.
  – At DARPA ITO Data Intensive Systems PI Meeting, Del Mar, CA, February 1998.

- ”New Research Topics in Computer Architecture”.
  – At Universidad de Zaragoza, Zaragoza, Spain, June 2002.

- ”A Framework for Dynamic Energy Efficiency and Temperature Management”.
  – At Universitat Politecnica de Catalunya, Barcelona, December 2000.

- ”Upcoming Architectural Advances in DSM Machines and Their Impact on Programmability”.
  – At Institute for Scientific Computing, Aachen, Germany, August 1999.

- ”Scal-Tool: Pinpointing and Quantifying Scalability Bottlenecks in DSM Multiprocessors”.
  – At Dagstuhl Seminar, Dagstuhl, Germany, August 2002.
  – At National Center for Supercomputing Applications (NCSA), Urbana, IL May 1999.

- ”New Trends in Computer Architecture and the i-ACOMA Scalable Multiprocessor Project”.
  – At NEC Corporation, Fuchu City, Japan, September 1999.
  – At Waseda University, Tokyo, Japan, September 1999.
  – At University of Houston, Houston, TX, January 1999.
  – At Universidade de A Corunha, A Coruhna, Spain, December 1998.
  – At Universidade de Santiago, Santiago, Spain, December 1998.
  – At Universitat Politecnica de Catalunya, Barcelona, Spain, December 1998.
  – At New York University, NY, October 1998.
  – At DARPA, Washington, DC, September 1998.
  – At NSF, Washington, DC, September 1998.
  – At the National Center for Supercomputing Applications, Urbana, IL, May 1998.
  – At Intel Corporation, Hillsboro, OR, April 1998.
  – At VLSI Circuits Seminar, University of Illinois at Urbana Champaign, April 1998.

- ”Efficient Execution of Database Workloads under Deep Memory Hierarchies”.
  – At Pennsylvania State University, State College, PA, November 1998.
  – At Oracle Corporation, Redwood Shores, CA, February 1998.
  – At Hewlett Packard Laboratories, Palo Alto, CA, February 1998.

- ”New Results in the Illinois Aggressive COMA Multiprocessor Project”.
  – At Los Alamos National Laboratory, Los Alamos NM, May 1998.
  – At Hewlett Packard Laboratories, Palo Alto, CA, February 1998.
  – At Texas A&M University, College Station, TX, January 1998.
  – At Convex Computer, Dallas, TX, January 1998.
  – At Northwestern University, Evanston, IL, December 1997.
  – At University of Washington, Seattle, WA, October 1997.
  – At Carnegie-Mellon University, Pittsburgh, PA, October 1997.
  – At Sequent Computers, Hillsboro, OR, April 1997.
  – At Silicon Graphics, Mountain View, CA, January 1997.
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, November 1996.

- ”Exploiting Billion-Transistor Chips for Multiprocessing”.
  – At IBM T.J. Watson Research Center, Yorktown Heights, NY, December 1997.
  – At Reflections/Projections ACM Student Chapter Conference, Urbana, IL, October 1997.

- ”The Illinois Aggressive COMA Multiprocessor”.
  – At Department of Computer Science, Tsinghua University, Beijing, China, January 1997.
  – At University of California-Berkeley, Berkeley, CA, February 1996.
  – At Stanford University, Stanford, CA, February 1996.
  – At Tandem Computers, Cupertino, CA, August 1995.
  – At SUN Microsystems, Mountain View, CA, August 1995.
  – At Universidad Politecnica de Valencia, Valencia, Spain, June 1995.
  – At Universite Paul Sabatier, Toulouse, France, June 1995.
  – At Intel Scalable Systems Division, Intel Corporation, Beaverton, OR, May 1995.

– At IBM T.J. Watson Research Center, Yorktown Heights, NY, February 1995.
– At Digital Equipment Corporation, Hudson, MA, February 1995.
– At Universitat Politecnica de Catalunya, Barcelona, Spain, December 1994.

- "The Performance of the Cedar Multistage Interconnection Network".
  – At Universitat Politecnica de Catalunya, Barcelona, Spain, December 1993.

- "The Cache Performance of Multiprocessor Operating Systems".
  – At Hewlett-Packard, Cupertino, CA, May 1992.
  – At Silicon Graphics Inc., Mountain View, CA, January 1992.
  – At SUN Microsystems Computer Corp., Palo Alto, CA, October 1991.

Conference Organization. Steering Committee

Dec 17	-	Dec 20	IEEE/ACM International Symposium on Microarchitecture (MICRO).
Jul 05	-	pres.	IEEE/ACM International Symposium on Computer Architecture (ISCA).
Jul 05	-	pres.	IEEE International Symposium on High-Performance Computer Architecture (HPCA).
Apr 06	-	Feb 08	ACM Symposium on Principles and Practice of Parallel Programming (PPoPP).
Sep 05	-	Oct 07	IEEE/ACM International Conference on Parallel Architectures and Compilation Techniques (PACT).
Aug 14	-	Aug 18	PACT.

Conference Organization. Chair

- Program Chair. The 23rd International Conference on Parallel Architectures and Compilation Techniques (PACT), Edmonton, Canada, August 2014.
- Program Chair. The 39th International Symposium on Computer Architecture (ISCA), Portland, OR, June 2012.
- Vice-General Chair. IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips), 2008-present.
- General Co-Chair. International Conference on Network and Parallel Computing (NPC), Shanghai, China, October 2008.
- Technical Papers Co-Chair. IEEE/ACM International Conference for High Performance Computing, Networking, Storage, and Analysis (SC07), Reno, NV, November 2007.
- General Chair. ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), New York, NY, March 2006.
- Program Chair. IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture Conferences, January-February 2006.
- General Chair. International Conference on Parallel Architectures and Compilation Techniques (PACT), Saint Louis, MO, September 2005.
- Program Chair. The 11th International Symposium on High-Performance Computer Architecture (HPCA), San Francisco, CA, February 2005.
- Architecture Area Chair. International Conference for High Performance Computing Networks and Storage (SC03), Phoenix, AZ, November 2003.
- Program Vice-Chair for Architecture. The 17th International Parallel and Distributed Processing Symposium (IPDPS), Nice, France, April 2003.
- Vice-Chair of Architecture. The 2001 International Conference on Parallel Processing (ICPP), Valencia, Spain, September 2001.
- General Co-Chair. The 6th International Symposium on High-Performance Computer Architecture (HPCA), Toulouse, France, January 2000.

- Minitrack Organizer. Minitrack on Scalable Shared-Memory Architectures. The 28th Hawaii International Conference on System Sciences (HICSS), Hawaii, January 1995.

Conference Organization. Program Committee

– International Symposium on Computer Architecture (ISCA): 2021, 2020 (external), 2019 (external), 2017, 2016 (external), 2015 (external), 2013, 2011, 2010, 2009, 2008, 2007, 2006, 2004, 2001.
– International Symposium on High Performance Computer Architecture (HPCA): 2019, 2018, 2017, 2016 (external), 2015, 2012, 2011, 2010, 2009, 2008, 2006, 2004, 2003, 2002, 2001, 1999, 1998.
– International Symposium on Microarchitecture (MICRO): 2021 (external), 2020 (external), 2019 (external), 2017 (external), 2016 (external), 2015, (external), 2012 (external), 2004, 2003.
– International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS): 2020 (external), 2018 (external), 2017 (external), 2016 (external), 2015 (external), 2014 (external), 2012 (external), 2011 (external), 2010 (external).
– International Conference on Parallel Architectures and Compilation Techniques (PACT): 2018 (external), 2017 (external), 2016, 2011, 2000.
– IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture Conferences: May-June 2021, May-June 2020, May-June 2015, May-June 2013, May-June 2012, January-February 2010, January-February 2008.
– International Conference for High Performance Computing Networks and Storage (SC): 2010, 2008, 2005, 2002.
– International Conference on High Performance Embedded Architectures and Compilers (HIPEAC): 2008.
– Symposium on Principles and Practice of Parallel Programming (PPoPP): 2005.
– Industrial Perspectives on Challenges for Next-Generation Computer Systems, International Symposium on High-Performance Computer Architecture (HPCA): 2005.
– Publications Chair. International Conference on Parallel Architectures and Compilation Techniques (PACT): 2004.
– International Conference on Supercomputing (ICS): 2003, 1999, 1997, 1996.
– International Parallel and Distributed Processing Symposium (IPDPS): 2002, 2001, 1998.
– Finance Chair. International Conference on Parallel Architectures and Compilation Techniques (PACT): 2001.
– Tutorials Chair. International Symposium on Computer Architecture (ISCA): 2001.
– Publicity Chair. International Conference on High Performance Computing (HIPC): 2000.
– International Conference on Parallel Processing (ICPP): 2000, 1999, 1998, 1997.
– International Conference on High Performance Computing (HIPC): 1999.
– Symposium on the Frontiers of Massively Parallel Processing: 1999, 1996.
– Workshops Chair. International Symposium on Computer Architecture (ISCA): 1998.
– Sigmetrics Conference: 1998.
– Workshops and Tutorials Chair. International Symposium on High-Performance Computer Architecture (HPCA): 1998.
– Registration Chair. International Computer Performance and Dependability Symposium (ICPDS): 1996.
– International Conference of the Chilean Computer Science Society (ICCCSS): 1995.
– International Conference on Distributed Computing Systems (ICDCS): 1995.
– International Computer Performance and Dependability Symposium (ICPDS): 1995.
– International Conference on Distributed Computing Systems (ICDCS): 1994.
– Registration Chair. International Symposium on Computer Architecture (ISCA): 1994.

Workshop Organization. Chair

- Program Co-Chair. Workshop on "Machine Learning, Artificial Intelligence, and Multi-Domain Operating Environment", Board on Army Research and Development, National Academies Study, May 2020 and August 2020.
- Program Co-Chair. NSF Workshop on "Inter-Disciplinary Research Challenges in Computer Systems", Williamsburg, VA, March 2018.
- Program Co-Chair. Workshop on "Managing Overprovisioned Processors", Salt Lake City, UT, March 2014.
- Program Chair. "2013 Illinois Symposium on Parallelism: Current State of the Field and the Future", Urbana, IL, September 2013.
- Program Co-Chair. Workshop on Advancing Computer Architecture Research (ACAR). "What Now in ILP Research?", Seattle, WA, September 2010.

- Program Co-Chair. Workshop on Advancing Computer Architecture Research (ACAR). "Failure is not an Option: Popular Parallel Programming", San Diego, CA, February 2010.

- Program Co-Chair. Intel/Microsoft/Illinois/Berkeley Universal Parallel Computing Research Center (UPCRC).
  – Workshop on Architecture, Santa Clara, CA, August 2011.
  – Workshop on Power Issues, Urbana, IL, April 2011.
  – Workshop on Architectures for Fine-Grain Synchronization, Redmond, WA, August 2010.
  – Workshop on Compilation for Block-Based Architectures, Urbana, IL, March 2010.
  – Workshop on Multicore Architectures for Programmability, Hillsboro, OR, August 2009.
  – Workshop on Multicore Computer Architecture for 2015, Urbana, IL, February 2009.
  – Workshop on Computer Architecture, Santa Clara, CA, August 2008

- Program Co-Chair. "Indo-US Workshop on Parallelism and the Future of High-Performance Computing", Bangalore, India, January 2010.

- Program Co-Chair. "First Workshop on Architectural and System Support for Improving Software Dependability" (ASID). In conjunction with ASPLOS-XII, San Jose, CA, October 2006.

- Program Co-Chair. "Second Workshop on Memory Performance Issues" (WMPI 2002). In conjunction with ISCA-29, Achorage, Alaska, May 2002.

- Program Co-Chair. "First Workshop on Memory Performance Issues" (WMPI 2001). In conjunction with ISCA-28, Goteborg, Sweden, June 2001.

- Program Co-Chair. "Ninth Workshop on Scalable Shared Memory Multiprocessors". In conjunction with ISCA-27, Vancouver, June 2000.

- Program Co-Chair. "Eighth Workshop on Scalable Shared Memory Multiprocessors". In conjunction with ISCA-26, Atlanta, GA, May 1999.

- Program Co-Chair. "Seventh Workshop on Scalable Shared Memory Multiprocessors". In conjunction with ISCA-25, Barcelona, June 1998.

- Program Co-Chair. "Fourth Workshop on Computer Architecture Evaluation Using Commercial Workloads". In conjunction with HPCA-7, Monterrey, Mexico January 2001.

- Program Co-Chair. "Third Workshop on Computer Architecture Evaluation Using Commercial Workloads". In conjunction with HPCA-6, Toulouse, France January 2000.

- Program Co-Chair. "Second Workshop on Computer Architecture Evaluation Using Commercial Workloads". In conjunction with HPCA-5, Orlando, January 1999.

- Program Co-Chair. "First Workshop on Computer Architecture Evaluation Using Commercial Workloads". In conjunction with HPCA-4, Las Vegas, February 1998.

- Program Chair. Birds-of-a-Feather Session on "Future Machine Architecture and Organization", at the National Computational Science Alliance (NCSA) Alliance'98, Urbana, IL, April 1998.

Workshop Organization. Program Committee

– Workshop on Near-Threshold Computing (WNTC): 2015, 2012.
– Workshop on Determinism and Correctness in Parallel Programming (WODET): 2013.
– Workshop on Hardware Support for Parallel Program Correctness: 2011.
– Workshop on System Effects of Logic Soft Errors (SELSE): 2007, 2006.
– Workshop on Multithreaded Architectures and Applications (MTAAP): 2007.
– Workshop on Power-Aware Computer Systems (PACS): 2003.
– Workshop on Multithreaded Execution, Architecture and Compilation (MTEAC): 2002, 2001, 2000, 1999.
– Workshop on Intelligent Memory Systems: 2000.

Tutorials and Short Courses

- Tutorial on "MCAt: Combining Machine Learning and Control Theory for Computer Architecture" at International Symposium on Microarchitecture (MICRO), October 2019, 1/2 day, http://iacoma.cs.uiuc.edu/mcat/.
- Course on "Parallel Computer Architecture Concepts", at International Spring School on High Performance Computing, San Sebastian/Donostia, Spain, April 2018. 5.25 hours.
- Course on "Modern Shared-Memory Parallel Computer Architecture", at Beihang University, Beijing, China, December 2012. 12 hours.
- Course on "High Performance Computing Architectures – Trends and Directions", at UIUC Course on High Performance Computing, Singapore, June 2010.
- "Parallel@Illinois Symposium at Singapore", Singapore, June 2010.
- Course on "Multiprocessor Architectures for Speculative Multithreading", at Fourth International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems (ACACES), L'Aquila, Italy, July 2008, one week.
- Course on "Boosting Machine Performance with Thread-Level Speculation", at Cursos de Verano, Universidad Complutense de Madrid, El Escorial, Spain, July 2004.
- Course on "New Technologies in Computer Architecture", Universidad de Zaragoza, Spain, June 2002.
- Tutorial on "Performance Modeling Using Hardware Counters", International Symposium on High-Performance Computer Architecture (HPCA), Toulouse, France, January 2000.
- Course on "Scalable Shared-Memory Multiprocessors", at Universitat Politecnica de Catalunya, Barcelona, Spain, July 1998.
- Tutorial on "Scalable Shared-Memory Multiprocessors: Architecture and Implementation Issues", at VII Jornadas de Paralelismo, Santiago, Spain, September 1996.

Panels Organized

- "Is There Research Funding Beyond Machine Learning and Quantum?", International Symposium on Computer Architecture (ISCA), June 2021.
- "How Do We Make HPCA Serve the Community Better", International Symposium on High Performance Computer Architecture, February 2019.
- "Broadening Computer Architecture Research: Embracing New Areas to Keep the Field Vibrant", International Symposium on Computer Architecture, June 2011.
- "Extreme Scale Computing: Challenges and Opportunities", International Symposium on High-Performance Computer Architecture and International Conference on Principles and Practice of Parallel Programming, Bangalore, India, January 2010.
- "High-Performance Architecture Research", Indo-US Workshop on Parallelism and the Future of High-Performance Computing, Bangalore, India, January 2010.
- "Speculative Multithreading Architectures", Minipanel at International Symposium on Computer Architecture, Austin, TX, June 2009.
- "How to Build a Useful Thousand-Core Manycore System?", IEEE International Parallel and Distributed Processing Symposium (IPDPS), Rome, Italy, May 2009.
- "Multi-Core and Many-Core: the 5 to 10 Year View", IEEE Symposium on Low-Power and High-Speed Chips, Yokohama, Japan, April 2009.
- "Wish List: Architectural Support and Tool Infrastructure for Improving Software Dependability", Workshop on Architectural and System Support for Improving Software Dependability (ASID), in conjunction with ASPLOS-XII, San Jose, CA, October 2006.

- ”An Agenda for Computer Architecture Research on Hardware Complexity”, Workshop on Complexity-Effective Design (WCED), in conjunction with ISCA-33, Boston, MA, June 2006.
- ”Soft Error Rate (SER) Scaling Trends”, Workshop on System Effects of Logic Soft Errors (SELSE), Urbana-Champaign, IL, April 2006.
- ”New Technologies in Computer Architecture”, Dagstuhl Seminar on Performance Analysis and Distributed Computing (PADC), Dagstuhl, Germany, August 2002.
- ”What’s the Most Critical Challenge is Supporting Multimedia Applications”, The 2001 International Conference on Parallel Processing (ICPP), Valencia, Spain, September 2001.
- ”Designing Scalable Shared-Memory Multiprocessors Using Commodity Microprocessors and OS: NUMA vs COMA Implementation”, Fifth Workshop on Scalable Shared-Memory Multiprocessors, Santa Margherita, Italy, June 1995.

Participation in Panels

– ”Demystifying Grad School”, The Third Young Architect Workshop (YArch), Virtual, April 2021.
– ”How to Get your Packet Seen?”, JOBS Workshop, Co-located with MICRO, Virtual, October 2020.
– ”Micro-Architectural Mitigations for Transient Execution Attacks”, Intel Side Channel Academic Program (SCAP) Workshop, Virtual, September 2020.
– ”Architecture and System for Big Data Processing”, Workshop on Architectures and Systems for Big Data (ASBD), Minneapolis, MN, June 2014.
– ”Future Applications and Challenges for NTC”, Workshop on Near-threshold Computing, Minneapolis, MN, June 2014.
– ”The Future of Parallelism”, 2013 Illinois Symposium on Parallelism: Current State of the Field and the Future, Urbana, IL, September 2013.
– ”Research Directions for 21st Century Computer Systems”, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), Houston, TX, March 2013.
– ”Future of Computing Systems”, IBM T.J. Watson Research Center, Yorktown Heights, NY, February 2013.
– ”Is Reliability the Main Roadblock to Ultra-Low Voltage Operation?”, Workshop on Near-threshold Computing (WNTC), Vancouver, Canada, December 2012.
– ”Many Core – Does It Work?”, 8th Workshop on Duplicating, Deconstructing, and Debunking (WDDD), Austin, TX, June 2009.
– ”How to Place Students in Top-5 Departments”, Department of Computer Science, UIUC, April 2009.
– ”Silicon Errors in Modern Integrated Circuits: What are the Main Threats”, Third Workshop on System Effects of Logic Soft Errors (SELSE-III), Austin, IL, April 2007.
– ”Chip Design in the Nano Era”, International Conference on Computer Aided Design (ICCAD), San Jose, CA, November 2005.
– ”What Are the Important Research Challenges in Temperature-Aware Computer Systems?”, Second Workshop on Temperature-Aware Computer Systems, Madison, WI, June 2005.
– ”Current and Future Processors”, Cursos de Verano, Universidad Complutense de Madrid, El Escorial, Spain, July 2004.
– ”Research Challenges for the Architecture Community in Temperature-Aware Design”, First Workshop on Temperature-Aware Computer Systems, Munich, Germany, June 2004.
– ”New Architectural Technologies”, DOE Salishan High Speed Computing Conference, Salishan Lodge, Gleneden Beach, OR, April 2004.
– ”What does the Future Hold for Parallel Languages?”, The 16th International Workshop on Languages and Compilers for Parallel Computing, College Station, TX, October 2003.
– ”Future Architectures and Programming Models for High Performance Computing”, International Symposium on Principles and Practice of Parallel Programming (PPoPP), San Diego, June 2003.
– ”Research in Computer Architecture”, XII Jornadas Nacionales de Paralelismo, Valencia, Spain, September 2001.
– ”Microprocessor Design Beyond the PC Era: Is There Room for Innovation?”, 15th International Parallel and Distributed Processing Symposium (IPDPS), San Francisco, April 2001.
– ”What Tools Do We Use to Evaluate Future Memory Systems?”, Third Workshop on Computer Architecture

Evaluation Using Commercial Workloads, Toulouse, France, January 2000.
– "Findings of the Petaflop Workshops", The 7th IEEE Symposium on the Frontiers of Massively Parallel Processing (Frontiers'99), Annapolis, MD, February 1999.
– "Issues in Petaflop Machines", The Third PetaFlop Workshop (TPF-3), Annapolis, MD, February 1999.
– "Cooperation Between Industry, Academia and Government to Make Commercial Applications Widely Available", 2nd Workshop on Computer Architecture Evaluation Using Commercial Workloads, Orlando, FL, January 1999.
– "Microbenchmarks: Risk versus Utility", Workshop on Performance Analysis and its Impact on Design (PAID), Barcelona, June 1998.
– "The First Course: Bottom-Up or Top-Down? Which is More Effective?", Fourth Workshop on Computer Architecture Education, Las Vegas, NV, January 1998.
– "Do Academics Require Access to DBMS Source Code in Order To Do Effective Research in the Area of Computer Architecture for Commercial Workloads?", First Workshop on Computer Architecture Evaluation Using Commercial Workloads, Las Vegas, NV, January 1998.
– "Multiprocessor Applications for IRAM", First Workshop on Mixing Logic and DRAM: Chips that Compute and Remember, Denver, CO, June 1997.
– "Paths to the Petaflops Architecture", The 6th Symposium on the Frontiers of Massively Parallel Computation (Frontiers'96), Annapolis, Maryland, October 1996.
– "Shared-Disk, Shared-Nothing, and Shared-Memory Architectures", First Intel Server Forum, Hillsboro OR, June 1996.
– "What are the Minimal Elements of a Computer Engineering or Computer Science Curriculum?", 2nd Annual Workshop on Computer Architecture Education, San Jose, California, February 1996.
– "Hot Research Topics in Processor Architecture and in Shared Memory Multiprocessor Architecture", 1st Workshop on Computer Architecture, Paris, France, June 1995.

Talks at Workshops

– "Thwarting Microarchitectural Replay Attacks", at Program Meeting, Hardware Security Research Program, Semiconductor Research Corporation (SRC), December 2020, June 2021.
– "Building Effective Defenses into Processors", at Intel Side Channel Academic Program (SCAP) Workshop, Virtual, September 2020.
– "A Secure Directory to Defeat Directory Side-Channel Attacks", at Intel Side Channel Academic Program (SCAP) Workshop, Hillsboro, OR, June 2019.
– "AutoPersist: A Java Framework to Program Non-Volatile Memory without Pain", at Runtimes in the Cloud, Phoenix, AZ, June 2019.
– "The Future of Computing: Secure Computing", at Future of Computing Open Mic Night, Phoenix, AZ, June 2019.
– "WiP: Cross-Core Prime+Probe Attacks on Non-inclusive Caches", at Workshop on Hardware and Architectural Support for Security and Privacy (HASP), June 2018.
– "Toward Extreme-Scale Shared-Memory Architectures", at Workshop on Perspectives of the Future of Computing, Gotheburg, Sweden, May 2018.
– "Defending Against Information Leakage: Computer Architecture Aspects", at NSF Workshop on Side and Covert Channels in Computing Systems, Washington, DC, March 2018.
– "Architectural Support for Novel Computing Paradigms", at Huawei-Illinois Workshop, Champaign, IL, October 2017.
– "What the Parallelism Center Accomplished", at 2013 Illinois Symposium on Parallelism: Current State of the Field and the Future, Urbana, IL, September 2013.
– "Parameter Variation at NT Voltage: The Power Efficiency versus Resilience Tradeoff", at DARPA PERFECT Program Meeting, Arlington, VA, February 2013.
– "The Illinois Parallelism Center", at Microsoft Faculty Summit, Seattle, WA, July 2012.
– "Toward Programmable Extreme Scale Computing", NSF/CISE Workshop on Cross-Layer Power Optimization and Management (CPOM), Los Angeles, CA, February 2012.
– "Thrifty: An Exascale Architecture for Energy-Proportional Computing", at Exascale Research Meeting, DOE Office of Advanced Scientific Computing Research, San Diego, CA, March 2011.
– "Accelerating Single-Thread Execution with Low Design Complexity: The BubbleWrap Approach", at Workshop on Advancing Computer Architecture Research (ACAR), What Now in ILP Research?, Seattle, WA, Sept. 2010.
– "Update on the Bulk Multicore Architecture", at Universal Parallel Computing Research Center (UPCRC) and Illinois Intel Parallelism Center (I2PC) Summits and Workshops: Santa Clara, CA (August 2008); Urbana, IL (February 2009); Hillsboro, OR (August 2009); Urbana, IL (March 2010); Seattle, WA (August 2010); Urbana, IL

(April 2011); Santa Clara, CA (August 2011); Hillsboro, OR (December 2011); Seattle, WA (July 2012); Santa Clara, CA (August 2012); Urbana, IL (September 2013).

– "The Architecture Needs to be Designed for Programmability", at Workshop on Advancing Computer Architecture Research (ACAR), Failure is not an Option: Popular Parallel Programming, San Diego, CA, February 2010.
– "High-Speed, Transparent, Scalable Checkpointing", at Intel Workshop on New Memory Technologies, Hillboro, OR, January 2010.
– "Simple Architectural Support to Check for Determinism", at Workshop on Determinism, Seattle, WA, December 2009.
– "The Bulk Compiler", Intel/Microsoft/Illinois/Berkeley UPCRC Workshop on Multicore Architectures for Programmability, Hillsboro, OR, August 2009.
– "Extreme Scale Architectures for Programmability", at DARPA-IPTO Workshop on Ubiquitous High Performance Computing, Stanford, CA, August 2009.
– "High-Performance Parallel Computer Architectures", at Workshop on Careers in High Performance Systems Mentoring, Urbana, IL, July 2009.
– "Multiprocessor Architectures for Programmability", at DARPA-IPTO Workshop on Exascale Ubiquitous High Performance Computing, University of Notre Dame, IN, April 2009.
– "The Bulk Multicore Architecture for Programmability", at Intel/Microsoft/Illinois/Berkeley UPCRC Workshop on Multicore Computer Architecture for 2015, Urbana, IL, February 2009.
– "The Bulk Multicore Architecture for Programmability", at Intel/Microsoft/Illinois/Berkeley UPCRC Workshop on Computer Architecture, Santa Clara, CA, August 2008.
– "How Do We Use 50-Billion Transistors on a Chip?", at Workshop on The 50 Billion Transistor Challenge, IBM T.J. Watson Research Center, Yorktown Heights, NY, July 2008.
– "An Updated Evaluation of ReCycle", at Workshop on Duplicating, Deconstructing, and Debunking, Beijing, China, June 2008.
– "Speculative Multithreaded Architectures", at Workshop on Architectures and Compilers for Multithreading, Indian Institute of Technology, Kanpur, India, December 2007.
– "Terascale-Level Multicore Processor Architectures: Promises and Roadblocks", at Workshop on Terachip Codesign, Defense Science Research Council (DSRC), Arlington, VA, October 2007.
– "Colorama: Supporting the Data-Centric Synchronization Model", at Workshop on Directions in Multi-Core Processor Research, Microsoft Research, Redmont, WA, January 2007.
– "Metrics for Processor Complexity", at Workshop on Complexity-Effective Design (WCED), in conjunction with ISCA, June 2005.
– "Modern Rollback Techniques", at DARPA-Sponsored Information Science and Technology (ISAT) Study on Law of Large Numbers System Design, Menlo Park, CA, February 2005.
– "New Architectural Technologies for Shared-Memory Systems", at DOE Salishan High Speed Computing Conference, Salishan Lodge, Gleneden Beach, OR, April 2004.
– "The FlexRAM Intelligent Memory System", at the Workshop on the Implementation of Multi-PIM Systems (WIMPS), Bodega Bay, CA, February 2002.
– "Hardware for Speculative Parallelization in High-End Multiprocessor", at The Third PetaFlop Workshop (TPF-3), Annapolis, MD, February 1999.
– "New Multithreading Architectures", at Internal IBM Workshop on Next Generation Processor Architectures, IBM Rochester, Rochester, MN, September 1998.
– "Hardware for Speculative Parallelization in Large- and Small-Scale Multiprocessors", at Seventh Workshop on Scalable Shared Memory Multiprocessors, Barcelona, June 1998.
– "Compiler Support for Data Forwarding in Scalable Shared-Memory Multiprocessors", at Seventh Workshop on Scalable Shared Memory Multiprocessors, Barcelona, June 1998.
– "Computer Architecture Education at the University of Illinois", at 5th Annual Workshop on Computer Architecture Education, Barcelona, Spain, June 1998.
– "COTS-Based Route to Petaflops Systems", at Petaflops Systems Operations Working Review (POWR), Bodega Bay, CA, June 1998.
– "FlexRAM: Advanced Intelligent Memory", at Data Intensive Computing Systems, DARPA PI Meeting, Del Mar, CA, February 1998.
– "How Processor-Memory Integration Affects the Design of DSMs", at First Workshop on Mixing Logic and DRAM: Chips that Compute and Remember, Denver, CO, June 1997.
– "A COTS-Based Petaflops Design", at 1997 Petaflops Algorithms Workshop (PAL'97), Williamsburg, VA, April 1997.

– "The Illinois Aggressive Cache Only Memory Architecture Multiprocessor", at Workshop on the Petaflop Frontier, Annapolis MD, October 1996.
– "The Illinois Aggressive Cache Only Memory Architecture Multiprocessor", at First Intel Server Forum, Hillsboro OR, June 1996.
– "The Illinois Aggressive Cache Only Memory Architecture Multiprocessor", at Petaflops Architecture Workshop (PAWS'96), Oxnard CA, April 1996.
– "Computer Architecture Education at the University of Illinois: Current Status and Some Thoughts", at 2nd Annual Workshop on Computer Architecture Education, San Jose, California, February 1996.
– "The Illinois Aggressive COMA Multiprocessor", at 1st Workshop on Computer Architecture, Paris, France, June 1995.
– "Evaluating the Benefits of Cache-Affinity Scheduling in Shared-Memory Multiprocessors", at Third Workshop on Scalable Shared-Memory Multiprocessors, San Diego, CA, May 1993.
– "The Cache Behavior of Shared Data in Cache-Coherent Multiprocessors", at First Workshop on Scalable Shared Memory Multiprocessors, Seattle, WA, May 1989.

Participation in Other Workshops and Meetings

– ISAT/DARPA "DOPLR: Data-Oblivious Interdisciplinary Representation", Virtual, Oct. 2020 - May 2021.
– "ARM Research Summit 2020", Virtual, September 2020.
– "Workshop on Digital Computing to Overcome the Limitations of Moore's Law", San Francisco, CA, May 2018.
– "International Roadmap for Devices and Systems (IRDS) Fall Workshop", McLean, VA, November 2017.
– "ARM Research Summit", Cambridge, UK, September 2016.
– "Nanotechnology-Inspired Information Processing Systems Workshop", Washington, DC, August 2016.
– "Computing Beyond 2025 Summit", Argonne National Laboratory, August 2016.
– "Arch2030: A Vision of Computer Architecture Research over the Next 15 Years Workshop", Seoul, Korea, June 2016.
– "CCC Symposium on Computing Research Addressing National Priorities and Societal Needs", Washington, DC, May 2016.
– "Computing Innovation Fellows (CIFellows) Workshop", San Francisco, CA, May 2014.
– "A Day at Technion", Technion, Haifa, Israel, June 2013.
– "30 Years of Parallel Computing at Argonne", Argonne National Laboratory, IL, May 2013.
– "DARPA PERFECT Program Meeting": Arlington, VA, February 2012; Arlington, VA, July 2013; Berkeley CA, January 2014.
– "DOE Exascale Research Conference": San Diego, CA, March 2011; Annapolis, MD, October 2011; Portland, OR, April 2012; Portland, OR, September 2012; Berkeley, CA, March 2013.
– "ACS Productivity Workshop", DOD, Ford Meade, MD, July 2011.
– "Universal Parallel Computing Research Center (UPCRC) and Illinois Intel Parallelism Center (I2PC) Summits and Workshops": Santa Clara, CA (August 2008); Urbana, IL (February 2009); Hillsboro, OR (August 2009); Urbana, IL (March 2010); Seattle, WA (August 2010); Urbana, IL (April 2011); Santa Clara, CA (August 2011); Hillsboro, OR (December 2011); Seattle, WA (July 2012); Santa Clara, CA (August 2012); Urbana, IL (September 2013).
– "DOE Salishan High Speed Computing Conference", Salishan Lodge, Gleneden Beach, OR, April 2010.
– "Google Day", San Jose, CA, July 2008.
– "Research@Intel Day", Mountain View, CA, June 2008.
– "DOE Salishan High Speed Computing Conference", Salishan Lodge, Gleneden Beach, OR, April 2008.
– "DOE/DOD Workshop on Emerging High Performance Architectures & Applications", Washington, DC, November 2007.
– "Workshop on Computer Academic/Industry Architecture Consortium (CAIAC)", Austin, TX, September 2007.
– "Microsoft Faculty Summit", Redmond, WA, July 2007.
– "DOE Salishan High Speed Computing Conference", Salishan Lodge, Gleneden Beach, OR, April 2006.
– "Computing Research Association (CRA) Conference on Grand Research Challenges: Revitalizing Computer Architecture Research", Monterey Bay, CA, December 2005.
– "Intel Multi-Core University Research Conference", Portland, OR, December 2005.
– "NSF-CISE Area Review. Area of Computer Architecture and Organization", NSF, May 2005.
– "DOE Salishan High Speed Computing Conference", Salishan Lodge, Gleneden Beach, OR, April 2005.
– "DARPA-Sponsored Information Science and Technology (ISAT) Study on Law of Large Numbers System Design", Menlo Park, CA, February 2005.

– ”Meeting of Lead PIs of Medium and Large Projects in the Information Technology Research (ITR) NSF Program”, Washington, June 2004.
– ”DOE Salishan High Speed Computing Conference”, Salishan Lodge, Gleneden Beach, OR, April 2004.
– ”Workshop on Software for Processor-In-Memory Based Parallel Systems”, San Jose, CA, March 2004.
– ”Science Case for Large-scale Simulation,” DOE Workshop, Washington, June 2003.
– ”Review Panel of the Programa Ramon y Cajal for Returning Scientists”, Government of Spain, Madrid, June 2003.
– ”Performance Analysis and Distributed Computing (PADC 2002)”, Dagstuhl Seminar, Dagstuhl, Germany, August 2002.
– ”Performance Engineering Technology & Research Sponsored Under the NSF Next Generation Software Program”, Austin, TX, February 2002.
– ”Workshop on the Implementation of Multi-PIM Systems (WIMPS)”, Bodega Bay, CA, February 2002.
– ”Review Panel of the Programa Ramon y Cajal for Returning Scientists”, Government of Spain, Madrid, September 2001.
– ”All Hands NCSA Meeting”, Urbana, IL, May 2001.
– ”NSF-CCR Workshop on Research Directions for Next-Generation Systems Design and Integration”, Seattle, WA, June 1999.
– ”NCSA Alliance Technical Working Meeting”, Oak Brooks, IL, May 1999.
– ”The Third PetaFlop Workshop (TPF-3)”, Annapolis, MD, February 1999.
– ”IBM Workshop on Next Generation Processor Architectures”, IBM Rochester, Rochester, MN, September 1998.
– ”Petaflops Systems Operations Working Review (POWR)”, Bodega Bay, CA, June 1998.
– ”Research Workshop between the University of Illinois at Urbana-Champaign and the Centre National de la Recherche Scientifique (CNRS) of France”, Urbana, IL, April 1998.
– ”National Computational Science Alliance (NCSA) Alliance’98 Conference”, Urbana, IL, April 1998.
– ”Petaflops Algorithms Workshop (PAL’97)”, Williamsburg, VA, April 1997.
– ”Workshop on the Petaflop Frontier”, Annapolis MD, October 1996.
– ”DARPA ITO General PI Meeting”, Dallas, TX, October 1996.
– ”DARPA Workshop on Performance Evaluation”, Washington DC, September 1996.
– ”NSF Experimental Research Workshop”, Washington DC, June 1996.
– ”Petasoft: Software for Petaflop Machines”, Bodega Bay CA, June 1996.
– ”First Intel Server Forum”, Hillsboro OR, June 1996.
– ”PetaFlops Architecture Workshop PAWS’96”, Oxnard CA, April 1996
– ”1st Workshop on Computer Architecture”, Paris, France, June 1995.

Graduated M.S. Students with Thesis

- Russell Daigle, Xiangfeng Chen, David Oesterreich, Alain Raynaud, Kittipong Mungnirun, Pedro Trancoso, Arun Sharma, Jovan Mitrevski, Jose Martinez, Zhenzhou Ge, Michael Huang, Yan Solihin, Jose Renau, Milos Prvulovic, Vinh Lam, James Tuck, Kuan Chen, Smruti Sarangi, Radu Teodorescu, Paul Sack, Brian Greskamp, Pablo Montesinos, Abdullah Muzahid, Ulya Karpuzcu, Shanxiang Qi, Rishi Agarwal, Marios Nicolaides, Ben Ahrens, Raghavendra Pothukuchi, Mengjia Yan, Tanmay Gangwani, Dimitrios Skarlatos, Ali Bohloolizamani, Yasser Shalabi, Azin Heidarshenas, Apostolos Kokolis, Antonio Franques-Garcia (”Fuzzy-Token: An adaptive MAC protocol for wireless network-on-chip”), Namrata Mantri (”Flexible Cuckoo Directory to Protect Against Side Channel Attacks”).

Postdoctoral Researchers

1. Sanyam Mehta, Oct 2014 - Aug 2015, from University of Minnesota.
2. Wonsun Ahn, Apr 2012 - Aug 2014, from University of Illinois.
3. Amin Ansari, Sep 2011 - Aug 2013, from University of Michigan.
4. Wei Liu, Aug 2001 - Aug 2006, from Tsinghua University, China; Now at Intel Corp.
5. Basilio Fraguela, Aug 2001 - Aug 2002, from Universidade A Coruna, Spain.

Visiting Scientists

1. Adrian Marruedo, Feb 2018 - Sep 2018, Universitat Politecnica de Catalunya, Spain.
2. Xavier Timoneda, Apr 2017 - Sep 2017, Universitat Politecnica de Catalunya, Spain.
3. Oscar Plata, Sep 2015 - Nov 2015, Universidad de Malaga, Spain.
4. Sonia Gonzalez, Sep 2015 - Nov 2015, Universidad de Malaga, Spain.
5. Sergi Abadal, May 2015 - Nov 2015, Universitat Politecnica de Catalunya, Spain.
6. Benjamin Sanhelices, Aug 2010 - Dec 2010, Universidad de Valladolid, Spain.
7. Lois Orosa, Sep 2009 - Dec 2009, Universidad de Santiago, Spain.
8. Norimasa Otsuki, Aug 2009 - Aug 2010, Renesas Technology, Japan.
9. Dario Suarez, May 2008 - Jul 2008, Universidad de Zaragoza, Spain.
10. Daniel Chaver, Jul 2002 - Aug 2002, Universidad Complutense de Madrid, Spain.
11. Keiji Kimura, Aug 2001 - Oct 2001, Waseda University, Japan.
12. Pedro Trancoso, Jul 2000 - Aug 2000, International College, Limassol, Cyprus.
13. Jaejin Lee, Aug 1999 - Dec 1999, Michigan State University, MI.
14. Paul Feautrier, Feb 1999 - May 1999, Universite de Versailles, Versailles, France.
15. Diego Llanos, May 1999 - Jul 1999, Universidad de Valladolid, Valladolid, Spain.
16. Josep Lluis Larriba-Pey, Apr 1996 - Sep 1996 and Jul 1997 - Sep 1997, Universitat Politecnica de Catalunya, Barcelona, Spain.

Teaching Activity

- Extensive teaching and advising experience at the undergraduate and graduate levels. Taught undergraduate- and graduate-level courses on computer architecture, computer organization, and logic design at UIUC.
- Was invited to talk about "Computer Architecture Education at the University of Illinois" at the 2nd, 4th, and 5th Workshop on Computer Architecture Education, February 1996, January 1998, and June 1998.
- Appeared in the local student newspaper Daily Illini under "Incomplete List of Teachers Ranked Excellent By Their Students" (Fall 1995, Spring 1995, Fall 1998, Spring 2018, Fall 2018, Spring 2019, Fall 2019, Spring 2021).
- Some of the courses taught were broadcasted to large off-campus audiences, both in the U.S. and in India.
- Organized the weekly Illinois-Intel Parallelism Center (I2PC) Distinguished Speaker Seminar (August 2011 - August 2013), and invited many Intel personnel to speak.
- Created a graduate-level weekly research seminar: "Research Topics in Advanced Computer Architecture".
- Developed semester-long special-topics courses: "Shared-Memory Multiprocessors: Architecture and Programming" (Spring 93), "Research Issues in New Processor and Memory Architectures" (Spring 01), and "Energy-Efficient Computer Architecture" (Fall 2016).

Other Major Service Outside UIUC

- Member, ISAT/DARPA "DOPLR: Data-Oblivious Interdisciplinary Representation", Oct. 2020 - May 2021.
- Vice Chair, IEEE Computer Society Fellow Evaluating Committee, 2020.
- Member, External Advisory Board of the WiPLASH European project: "Architecting More Than Moore - Wireless Plasticity for Massive Heterogeneous Computer Architectures", 2020-present.

- Member, External Review Committee of the Computer Science Ph.D. and M.S. programs, College of Computing, Georgia Institute of Technology, Fall 2018.
- Member, Selection Committee for the IEEE Harry Goode Award, 2016, 2017.
- Participant in many NSF and DARPA workshops, PI meetings, and program-conception meetings, including DARPA's "Data Intensive Systems", "Bio-Computation", "Polymorphous Computer Architectures", "High Productivity Computer Architectures", "Ubiquitous High Performance Computing", and "Power Efficiency Revolution for Embedded Computing Technology".
- Presented the outcome of Computing Community Consortium workshops to CCC, DOE, NSF, AFOSR, and NITRD.
- CCC-appointed liaison to guide the visioning workshops on "Charting the Future of Electronic Design Automation", March 2013, June 2013, and February 2014.
- Member of the Steering Committee, IEEE Computer Society Multicore, April 2013 - pres.
- Member of the IEEE Fellows Selection Committee, 2012, 2013, 2016.
- Member, Computing Innovation Fellows Selection Committee, CCC and CRA, 2010.
- Member, Search Committee for Editor-in-Chief of the Computer Architecture Letters (CAL) journal, 2005.
- Participant, Site Visit for NSF Expeditions in Computing, December 2015.
- Participant in many NSF Proposal Evaluation Panels: March 1996, November 1998, March 2000, July 2001, February 2002, February 2003, May 2004, August 2004, October 2007, April 2008, December 2008, April 2009, March 2010, December 2010, March 2011, March 2012, May 2013, June 2014.
- Member of the Advisory Board, Department of Electrical and Computer Engineering, University of Rochester, 2003-pres.
- Member of Enabling Technologies Team A, NSF's National Computational Science Alliance (NCSA) Partnership for an Advanced Computational Infrastructure (PACI), 1997 - 2004.
- I-ACOMA research project was selected as one of the "Eight Point-Design Studies" that DARPA, NSF, NSA and NASA supported in 1996, in a nationwide effort to accelerate the arrival of a petaflop-level machine.
- Regular referee for the major conferences and journals in computer architecture and parallel processing, and reviewer of books on computer architecture.

Major Service Inside UIUC

- Guest Speaker at the Video Celebration of Doctoral Graduates, Graduate College, UIUC, December 2020.
- Member, Computer Science Promotion and Tenure Committee, 2018-2021.
- Member, Graduate Student Mentoring Guidelines Working Group, College of Engineering, 2019.
- Member of the Advisory Board, IBM-Illinois Center for Cognitive Computing Systems Research, April 2016.
- Member, Search Committee for Associate Dean for Graduate, Professional, and Online Education, College of Engineering, March 2016.
- Member of College of Engineering Executive Committee (2002-2008) and Grievance Committee.
- Served in many committees at the College of Engineering and at the Department of Computer Science: Promotions and Tenure; Faculty Recruiting; Chairs and Professorships; Faculty and Staff Awards; Advisory; Distinguished Lecture and Departmental Seminar; Fellowships, Assistantships and Graduate Admissions; Computing and Technology Advisory; Task Force on Graduate Student Weekend; Courses and Curriculum; Undergraduate Study; Graduate Advising; Undergraduate Advising; TEI; Graduate Research Orientation; Standing Subcommittee on Engineering/Chemistry Liaison; Computer Affiliates Program; Search Committee for the Director of Budget and Resource Planning; CSL Computing and Networking; and CSRD Industrial Affiliates Program.

- Member, Computer Science Department Head Review Committee, 2015.
- Chair, Architecture, Compilers, and Parallel Computing Area, Department of Computer Science, 2004-2006, 2016-2017, 2020-pres.
- Member, Parallel Computing Institute (PCI) Growth Committee, 2013-pres.
- Host to many speakers and visitors invited to the Department of Computer Science.
- Participated and organized faculty retreats for the Computer Science Department, Computer Engineering, and College of Engineering.
- Participated in several Illinois Computer Science Alumni reunions across the nation.

Other Activities

- Consultant for several companies.
- Consultant for patent assessment. Member of the Round Table Group (RTG) Network of Patent Consultants.