

# XUEHAI QIAN

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## Research Interests

Computer architecture, Computer Arithmetic, Parallel programming

## Education

Sept. 2007 – Present	PhD Student
Computer Science Dept.	University of Illinois, Urbana-Champaign
Advisor:	Josep Torrellas
Sept. 2004 – July 2007	Master of Engineering in Computer Science
Institute of Computing Technology (ICT)	Chinese Academy of Sciences
Advisor:	Weiwu Hu (area: Computer Architecture)
Thesis: “ <i>Design and Implementation of x86 compliant floating point architecture</i> ”	
Sept. 2000 – July 2004	Bachelor of Engineering in Computer Science
School of Computer Science	Beijing University of Aeronautics and Astronautics (BUAA)
Thesis: “ <i>Optimization for Multimedia Applications based on the Multimedia Instruction Set Extension of Godson-2 Microprocessor</i> ”	

## Honors

2008 Nominated for the Microsoft Research Ph.D. Fellowship program by the CS Dept of UIUC  
2007 Andrew and Shana Laursen Fellowship, UIUC  
2007 Excellent M.S Dissertation ICT, CAS  
2006 NOKIA Scholarship ICT, CAS  
2006 All-around Excellent Student Award ICT, CAS  
2004 Excellent B.S Dissertation Award, BUAA  
2003 “Qian Changzhao,” Scholarship, BUAA  
2003 Renmin Scholarship, BUAA

## Publications

- [1] Xuehai Qian, He Huang, Hao Zhang, Junchao Zhang, Dongrui Fan. “*Design and implementation of floating point stack on general RISC architecture*” 15th Euromicro Conference on Parallel, Distributed and Network based Processing (PDP 2007). Naples, Italy, February 7-9, 2007 (Cited by *Microprocessor Report*, Nov. 3<sup>rd</sup>, 2008, Issue as one of the core papers in Godson-emulated x86 processor design)
- [2] Xuehai Qian, He Huang, Zhenzhong Duan, etc. “*Optimized register renaming scheme for stack - based x86 floating point operations*” ARCS'07 Architecture of Computing Systems. Swiss Federal Institute of Technology (ETH) Zurich, Switzerland. March 12-15, 2007 (acceptance ratio: 20/83=24%) (Cited by *Microprocessor Report*, Nov. 3<sup>rd</sup>, 2008, Issue as one of the core papers in Godson-emulated x86 processor design)
- [3] Xuehai Qian, Hao Zhang, Jingang Yang, etc. “*Circuit implementation of floating point range reduction for trigonometric functions*” 2007 IEEE International Symposium on Circuits and Systems. New Orleans. May 27-30, 2007

[4] Hao Zhang, Wei Lin, Xuehai Qian, Dongrui Fan, etc. “High bandwidth memory access pipeline” Chinese Journal of Computers (in Chinese)

[5] Hao Zhang, Xuehai Qian.”Self Modify Code Handling on Godson - X” Computer Engineering. (in Chinese)

## Research Experience

- August 2008 – Present: Research Assistant of IACOMA group  
Advisor: Josep Torrellas  
Topic: *Optimization of the execution of chunk-based system*  
This research is based on the previous work on chunk-based execution from IACOMA group (Bulk, BulkSC and Delorean), we are thinking and implementing the ideas on improving execution efficiency of chunk-based system.
  
- May 2008 – Aug. 2008: Research Intern in Microsoft Research, Redmond  
Mentor: Onur Mutlu  
Topic: *Development and extension of memory controller and interconnection simulator; analysis behavior of LiveSearch workload*
  - 1) We extended the previous work on fairness in memory controller to multiple-controller case, observed the memory access behavior in the extended architecture. After that we proposed and implemented new mechanisms to enhance fairness in multiple memory controllers, we plan to submit a comprehensive paper on fairness of memory controller based on this work and previous results.
  - 2) We incorporated an existing On-chip network simulator with memory system simulator used in MSR to investigate the behavior of on-chip network in the memory system, especially the fairness issue. Also, we developed simplified but efficient energy model to evaluate novel ideas on interconnection network design. This model abstracts away many details in router design but can quickly estimate the impact of the changes in network topology and algorithm on energy consumption of interconnect. This model will be used in future work from Microsoft on interconnects.
  - 3) Search is one of the most promising workload currently, we are trying to analyze the behavior of this workload and propose energy efficient architecture for the data-center computing. In this work, I obtained traces from the real LiveSearch engine using IDNA infrastructure (including TTTracer and Truscan). I was also involved in optimizing the ranking algorithms in LiveSearch engine and defining highly efficient instructions for accessing the data in high compressed format (for the purpose of reducing memory footprint) which is widely used in search engine.
  
- Nov. 2007 – May 2008: Fellowship student (worked in IACOMA group)  
Advisor: Josep Torrellas  
Topic: *Efficient Synchronization mechanism in multicore system*  
In this research, we tried to identify the cases of redundant synchronizations in parallel and multithreaded programs, and proposed hardware to eliminate them at runtime. In this way, the unnecessary stalls due to the synchronization can be eliminated.
  
- Aug. 2007 – Oct. 2008: Fellowship student (worked in OPERA group)  
Advisor: Yuanyuan Zhou  
Topic: *Concurrent software testing*  
We conducted a thorough investigation of the characteristics of concurrent program interleaving, and used the characteristics to guide efficient concurrent program testing. We found out the reason why some concurrency bugs have very low occurrence probability under uncontrolled execution. Based on the characteristics of interleaving, we proposed a new concurrent program testing scheme to effectively explore concurrent programs’ interleaving space and expose concurrency bugs.

- Mar. 2005 – Jun. 2007: Research Assistant  
Key Laboratory of Computer System and Architecture  
Institute of Computer Technology, Chinese Academy of Sciences

Topics:

1) *Research of the future architecture for Godson - 3 processor*

We considered two ways for Godson-3 architecture to accelerating the single task:

- a) Variable ISA: We can combine multiple one cycle instructions into one cycle complex instruction to achieve more computation throughput per cycle. First, compiler generate generic “simple” operations, then, it inspects nearby operations for combinations that may be optimized. After identified these optimization opportunity, the compiler adds new instruction and data path programming information. Finally, codes are re-generated using new instructions.
- b) Multi-processor clusters: The key technology behind this architecture is memory block re-assignment. Memory is divided into small blocks which can be routed so that they can be accessed by one of several nearby processor units. The data transfer overhead can be minimized.

2) *Implementation of x86 compliant processor and virtual machine*

(Described in a dedicated article in *Microprocessor Report* Nov. 3<sup>rd</sup>, 2008. “*Godson-3 Emulates x86, New MIPS-Compatible Chinese Processor Has Extensions for x86 Translation*”)

The aim of our group is to run x86 programs on the RISC Godson processor. The first approach is implementing a prototype full x86 compliant processor based on the core of Godson-2C (Godson-X). The second strategy is implementing a co-designed x86 virtual machine, namely Godson-VM. I have participated in the following tasks:

- a) Building a cycle-accurate simulator based on the simulator of Godson-2C processor. (in charge of the floating point unit design and architectural support related to x86 stack-based floating point register organization)
- b) Implementing stack-based x86 floating point structure on the original Godson architecture. (in charge)
- c) Debugging the simulator of the prototype processor so that it can boot unmodified Linux and Windows XP operating system for x86 machine. (main participant)
- d) Optimizing the architecture of Godson-X, mainly register renaming module and memory system. (main participant)
- e) Implementing the floating point computation circuits in Verilog, including floating point addition, multiplication, division, square root and transcendental functions such as sin, cos, tan, ftan, etc. (in charge)
- f) Building HW/SW co-designed x86 virtual machine based on modified Godson-2C core with some x86 related support. (main participant)
- g) Testing and verification of the design, at both architectural level and circuit level. (in charge of floating point part)

- Feb. 2004 – Jun. 2004: Visiting Student  
Key Laboratory of Computer System and Architecture  
Institute of Computer Technology, Chinese Academy of Sciences  
Advisor: Prof. Zhimin Tang (former member in ICT)

Topic: *Multimedia software optimization for Godson - 2C processor*

To enhance the performance of multimedia applications, the Godson-2C processor implements an extended multimedia instruction set. We analyzed the performance of multimedia workload on the Godson-2C processor using Mediabench and optimized the MPEG2 decoder and some processing cores for Multimedia Workload from Berkeley. The speedup to the MPEG2 decoder are 30% to 40% for different video streams. The optimization enabled the Godson-2C processor to play DVD streaming smoothly, note that the processor runs at a frequency of only 350MHz.

## Reference

Available upon request