

Xuehai Qian

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RESEARCH INTERESTS	Processor design, multiprocessor, cache coherence, memory consistency model, transactional memory, chunk-based system, distributed on-chip architecture and on-chip interconnect network.	
EDUCATION	University of Illinois, Urbana-Champaign (UIUC) , Urbana, IL USA Ph.D., Computer Science, Aug. 2007 to present <ul style="list-style-type: none">• Thesis Topic: <i>Bulk: Scalable and Efficient Architecture for Improved Programmability</i>• Adviser: Professor Josep Torrellas• Area of Study: Computer Architecture Institute of Computing Technology (ICT), Chinese Academy of Sciences (CAS) , Beijing, China M.S., Computer Engineering, Jul. 2007 <ul style="list-style-type: none">• Thesis Topic: <i>Design and Implementation of X86 Compliant Floating Point Architecture</i>• Adviser: Professor Weiwu Hu• Area of Study: Computer Architecture Beihang University (BUAA) , Beijing, China B.S., Computer Engineering, July 2004 <ul style="list-style-type: none">• With Honors in Engineering• Thesis Topic: <i>Optimization of Multimedia Applications using SIMD ISA Extension of Godson-2 Processor</i>	
AWARDS AND HONORS	University of Illinois, Urbana-Champaign <ul style="list-style-type: none">• Nominated for the IBM Ph.D Fellowship by Department of Computer Sciences (one of 2 nominees), 2011• Nominated for the Microsoft Research Ph.D Fellowship by Department of Computer Sciences (3 nominees), 2008• Andrew and Shana Laursen Fellowship, 2007 Institute of Computing Technology, CAS <ul style="list-style-type: none">• Outstanding Master Dissertation Award, 2007• NOKIA Fellowship, 2007• All-around Outstanding Student Award, 2006 Beihang University <ul style="list-style-type: none">• Distinguished Bachelor Dissertation Award, 2004• <i>QIAN Changzhao</i> Fellowship, 2003 (top one computer science student)• <i>People</i> Fellowship, 2003	

PUBLICATIONS

Xuehai Qian, Benjamin Fernandez and Josep Torrellas, "*BulkSMT: Designing SMT Processors for Atomic-Block Execution*". The 18th International Symposium on High Performance Computer Architecture (**HPCA**), Feb. 2012.

Xuehai Qian, Wonsun Ahn and Josep Torrellas, "*ScalableBulk: Scalable Cache Coherence for Atomic Blocks*". The 43rd Annual International Symposium on Microarchitecture (**MICRO**), Dec. 2010.

Xuehai Qian, He Huang, Hao Zhang, Junchao Zhang and Dongrui Fan, "*Design and Implementation of Floating Point Stack on General RISC Architecture*". The 15th Euromicro Conference on Parallel, Distributed and Network-based Processing (**PDP**), Feb. 2007. (Cited by **Microprocessor Report**, Nov. 3rd, 2008 as one of the core papers in Godson-emulated x86 processor design)

Xuehai Qian, He Huang, Zhenzhong Duan, etc., "*Optimized Register Renaming Scheme for Stack-based X86 Floating Point Operations*". 20th International Conference on Architecture of Computing Systems (**ARCS**), Mar. 2007. (Cited by **Microprocessor Report**, Nov. 3rd, 2008 as one of the core papers in Godson-emulated x86 processor design)

Xuehai Qian, Hao Zhang, Jingang Yang, etc., "*Circuit Implementation of Floating Point Range Reduction for Trigonometric Functions*". 2007 IEEE International Symposium on Circuits and Systems (**ISCAS**). May 2007.

Lei Liu, He Huang, **Xuehai Qian**, Zhimin Tang and Leijun Hu, "*Rainbow: On-The-Fly Log Reduction for Effective Memory Race Recording*". Journal of Computer Research and Development. Accepted. (in Chinese)

Hao Zhang and **Xuehai Qian**, "*Self Modify Code Handling on Godson-X*". Computer Engineering. Mar. 2008. (in Chinese)

RESEARCH
EXPERIENCE

University of Illinois, Urbana-Champaign, Urbana, IL USA

Graduate Research Assistant, I-Acoma group **Nov. 2007 to Present**
Advisor: Josep Torrellas

My research focuses on designing scalable and efficient architectures for improved programmability. Specifically, we focus on the architecture for atomic block and efficient implementation of sequential consistency. I work on the following projects:

- *ScalableBulk*: A cache coherence protocol for atomic block commit in lazy environment.
- *BulkSMT*: Supports atomic block execution in contexts in SMT.
- *Infrastructure*:
 1. A simulator for BulkSC architecture based on Simic and FeS2.
 2. A network model in SESC to evaluate scalable cache coherence protocol.
 3. Atomic block support for SMT in SESC.

Graduate Research Assistant, Opera group **Aug. 2007 to Oct. 2007**
Advisor: Yuanyuan (YY) Zhou

I analyzed the interleaving behavior of some parallel applications.

Microsoft Research, Silicon Valley, Mountain View, CA USA

Graduate Research Intern **May. 2011 to Aug. 2011**
Mentor: John Davis

The project is about DRAM De-duplication for the mem-cached applications. These applications require a lot of DRAM. The de-duplication can either reduce the DRAM requirement and save the energy or allow more data into the same DRAM and improve the performance. The initial application is the BING index file. I analyzed and understood the structure of the file and identified that most of the content is the delta locations. Then I proposed several algorithms to analyze and identify the redundancy in the delta location sequences. My schemes can reduce the data value stored by more than 50% and incurs limited meta data overhead. Currently we are trying to further reduce the meta data overhead.

Microsoft Research, Redmond, WA USA

Graduate Research Intern, Architecture Group **May. 2008 to Aug. 2008**
Mentor: Onur Mutlu

I extended the memory controller and on-chip network simulator and evaluated the performance of LiveSearch workload. More specifically, I worked on the following aspects:

- Extended the fairness memory controller to multiple-controller case and analyzed the memory access behavior in the extended architecture.
- Incorporated an on-chip network simulator with memory system simulator to investigate the behavior, especially fairness aspects, of the network in memory system.
- Developed a simple but effective energy model to quickly estimate the impact of the changes in network topology and routing algorithm on energy consumption.
- Collect traces from the real LiveSearch engine using IDNA infrastructure.

Institute of Computing Technology (ICT), CAS, Beijing, China

Research Assistant, Godson Project **Mar. 2005 to Jun. 2007**
Advisor: Prof. Weiwu Hu

I was mainly involved in the research and design of Godson-2 (single processor), Godson-X (X86 version of Godson-2) and Godson-3 (multi-core). I was working on the following projects:

- Godson-3: We evaluated two ideas for the processor, — variable ISA and multi-processor clusters.
- ScopeCC: Instead of hardware cache coherence, we proposed the alternative approach for the on-chip communication mechanism for many-core architecture. The system achieves similar performance as directory-based protocol but with much lower cost and complexity.
- Godson-X: (described in a dedicated article in *Microprocessor Report Nov. 3rd, 2008. "Godson-3 Emulates x86, New MIPS-Compatible Chinese Processor Has Extensions for x86 Translation"*) I was involved in simulator development, testing and validation. I was in charge of floating point architecture support. The main challenge is the stack-based floating point register organization, higher precision FP operation and special functions.

Visiting Student, Godson Project **Jan. 2004 to Jun. 2004**
Advisor: Zhimin Tang

Optimized some multimedia applications (i.e mpeg-2 decoder) and some kernels in MediaBench workload using SIMD ISA supported in Godson-2.

TEACHING
EXPERIENCE

- **Teaching Assistant**, *CS533: Parallel Computer Architecture*. UIUC
Spring 2010.
- **Guest Lecturer**, *CS533: Parallel Computer Architecture*. UIUC
Spring 2010, 2011, 2012.

TALKS

- *"DRAM De-Duplication for Bing"*
Microsoft Research, Silicon Valley. Mountain View, CA. Aug. 2011
- *"BulkSMT: Designing SMT Processors for Atomic-Block Execution"*
The 18th International Symposium on High Performance Computer Architecture (**HPCA**), Feb. 2012.
- *"ScalableBulk: Scalable Cache Coherence for Atomic Blocks in Lazy Environment"*
Beihang University. Beijing, Dec. 2010.
Tsinghua University. Beijing, Dec. 2010.
Institute of Computing Technology, Chinese Academy of Sciences. Beijing. Jan. 2011.
IBM Research - China. Beijing, Jan. 2011.
The 43rd Annual International Symposium on Microarchitecture (**MICRO**), Dec. 2010.
Universal Parallel Computer Research Center (UPCRC) Seminar, Mar. 2011.
- *"Optimized Register Renaming Scheme for Stack-based X86 Floating Point Operations"*, 20th International Conference on Architecture of Computing Systems (**ARCS**), Zurich, Switzerland, Mar. 2007.
- *"Design and Implementation of Floating Point Stack on General RISC Architecture"*, The 15th Euromicro Conference on Parallel, Distributed and Network-based Processing (**PDP**), Naples, Italy, Feb. 2007.

SERVICE

- Student Member of ACM and SIGARCH.
- External reviewer for ISCA, HPCA.
- Submission co-chair of ISCA 2012.

REFERENCES

- **Prof. Josep Torrellas**.
Advisor.
Department of Computer Sciences, UIUC.
torrellas@cs.uiuc.edu
- **Prof. Tao Li**.
Collaborator.
Department of Electrical and Computer Engineering,
University of Florida.
taoli@ece.ufl.edu
- **Dr. John Davis**.
Mentor in Microsoft Research, Silicon Valley.
john.d@microsoft.com

- **Prof. Onur Mutlu.**
Mentor in Microsoft Research, Redmond.
Department of Electrical and Computer Engineering, CMU.
onur@cmu.edu
- **Dr. Xiaowei Shen.**
Associate Director and CTO, IBM Research - China
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- **Dr. Jian Li.**
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