

Shanxiang Qi

University of Illinois at Urbana-Champaign
Department of Computer Science
4238 Siebel Center for Computer Sciences
201 N. Goodwin Avenue
Urbana, IL 61801

Tel.(Office): 217.244.2445
Tel.(Cell): 217.817.0125

Email: sqi2@uiuc.edu

RESEARCH INTERESTS

Computer architecture, compiler, parallel programming

EDUCATION

Sept. 2007 – Present
Computer Science Dept.
Advisor:

Ph.D. Student
University of Illinois at Urbana-Champaign
Prof. Josep Torrellas

Sept. 2007 – May 2010
Computer Science Dept.
Advisor:

M.S. in Computer Science
University of Illinois at Urbana-Champaign
Prof. Josep Torrellas

Thesis: "Tolerating asymmetric data races with minimal hardware support"

Sept. 2003 – July 2007
Computer Science Dept.

B.E. in Computer Science
Tsinghua University, Beijing, P.R.China

Thesis: "*The design and implement of the dynamic trace collection for the Linux file system*" (**Outstanding Thesis Award**)

RESEARCH EXPERIENCE

Jun. 2009 – Aug. 2009 Research Intern, Storage group, **IBM Almaden Research Center**
Menter: Leo Luan

Topic: Sequential Inter-file Pre-fetching

It is important and useful for applications, such as backup/archive software and search tools, to traverse a file system tree. These applications do not benefit fully from parallel I/Os because file data prefetching is only done after a file is read accessed. We design a mechanism for a file system to prefetch files for application that does directory-tree traversal. Our experiment shows that on IBM GPFS file system, we improved the throughput of tar application 10X from 60MB/sec to 600MB/sec.

Aug. 2007 - Present: Research Assistant, **University of Illinois at Urbana-Champaign**
Advisor: Prof. Josep Torrellas

Detecting and tolerating data races

We propose a new way to detect the data race in parallel programs. Our approach is based on hardware address signatures that summarize the locations accessed by the processors. We use signature and timestamp to detect the data race. I tested and analyzed the behavior of data races in several benchmarks.

We also proposed the first scheme to detect and tolerate asymmetric data races in hardware. The approach induces negligible execution overhead and requires minimal hardware modifications. Processor, cache coherence, and protocol messages remain unchanged. It makes a novel use of hardware address signatures to detect the asymmetric races.

Compiler support for chunk-based execution

We use compiler technology to improve our novel chunk-based execution architecture (Bulk, BulkSC and Delorean). In chunk-based architecture, it allows the compiler to reorder the instructions across the synchronization instruction within a chunk. I analyze the synchronization behavior in JAVA Hotspot compiler and decide where to cut the chunk. I also look at which compiler optimizations are useful to enhance the performance of our chunk-based execution architecture.

Redundant execution for speedup programs

This project uses redundant leader-checker execution model to speedup programs or save the power. I proposed a multiple-leader model to improve the performance.

Jan. 2006 - Jun 2007: Research Student, **Tsinghua University**

Advisor: Dr. Wei Xue, Prof. Weimin Zheng

Dynamic trace collections for the Linux file system - (2007.1 – 2007.6)

Developed VFS-Tracer, a dynamic trace collection based on the VFS level. VFS-Tracer can capture uniform traces for any file system, while running without modifying the file systems being traced. VFS-Tracer can dynamic capture traces without any change in a running file system. I have implemented and evaluated a prototype VFS-Tracer on Linux. Our evaluation shows a highly versatile system with dynamic loading and low overheads.

Improvement the partition method for parallel programs - (2006.1 – 2006.12)

We discovered that the partition in power system programs can be improved and widely used in other areas. I implemented the new partition algorithm for the program. Our result shows that with eight CPUs, the efficiency of our algorithm was about 70% higher than the original of METIS which is one of the families of Multilevel Partitioning algorithms.

PUBLICATION

- [1] Abdullah Muzahid, **Shanxiang Qi** and Josep Torrellas, Vulcan: Hardware Support for Detecting Sequential Consistency Violations in Programs Dynamically, Submitted for publication.
- [2] **Shanxiang Qi**, Abdullah Muzahid and Josep Torrellas, Swift: Dynamically Detecting and Tolerating IF-condition Data Races, Submitted for publication.
- [3] **Shanxiang Qi**, Norimasa Otsuki, Lois Orosa Nogueira, Abdullah Muzahid, and Josep Torrellas, Pacman: Tolerating Asymmetric Data Races with Minimal Hardware Support, The 18th International Symposium on High Performance Computer Architecture (**HPCA'12**), February 2012.
- [4] Cindy Xide Lin, Qiaozhu Mei, Yunliang Jiang, Jiawei Han, **Shanxiang Qi**, Inferring the Diffusion and Evolution of Topics in Social Communities, SNA-KDD Workshop 2011
- [5] Wonsun Ahn, **Shanxiang Qi**, Jae-Woo Lee, Marios Nicolaides, Xing Fang, Josep Torrellas, David Wong, and Samuel Midkiff,, BulkCompiler: High-Performance Sequential Consistency through Cooperative Compiler and Hardware Support, International Symposium on Microarchitecture (**MICRO'09**), December 2009.
- [6] Abdullah Muzahid, Dario Suarez, **Shanxiang Qi**, and Josep Torrellas, *SigRace: Signature-Based Data Race Detection*, 36th International Symposium on Computer Architecture (**ISCA '09**), June 2009.
- [7] Wei Xue, and **Shanxiang Qi**, *Multilevel Task Partition Algorithm for Parallel Simulation of Power System Dynamics* International Conference on Computational Science (**ICCS 2007**), May 2007.

AWARDS AND HONORS

- President of UIUC-CSSA (Chinese Students and Scholars Associations) - 2010-2011
- Outstanding bachelor's thesis in Tsinghua University- 2007
- Second Prize in Intel National Optimize Programming Contest - 2005
- Scholarship of Academic Excellence by Tsinghua University - 2005
- Bronze Medal in CMO(Chinese Mathematical Olympiad) – 2002&2003
- First Prize in National Competition in Mathematics – 2001&2002