

Smruti R. Sarangi

CONTACT INFORMATION	Siebel Center 4238 Computer Science Department 201 N. Goodwin Ave Urbana, IL - 61801 USA	<i>Phone:</i> (217) 369-1285 <i>Fax:</i> (217) 265-6582 <i>E-mail:</i> sarangi@cs.uiuc.edu http://iacoma.cs.uiuc.edu/~sarangi
RESEARCH INTERESTS	reliable processors, fault tolerance and verification methods, thread level speculative architectures, power management	
EDUCATION	University of Illinois at Urbana-Champaign, IL Ph.D. Candidate, Computer Science (Aug. 2002 - present)	
	University of Illinois at Urbana Champaign, IL M.S., Computer Science, Dec, 2004 (GPA 3.95/4.00)	
	Indian Institute of Technology, Kharagpur, India B.Tech, Computer Science, May 2002 (GPA 9.30/10.00)	
HONORS AND AWARDS	“Energy-Efficient Thread-Level Speculation on a CMP” selected in IEEE Micro Top picks. (top 13 papers in computer architecture in 2005)	
	David J. Kuck, Best MS thesis award in the department of computer science, UIUC in 2004.	
	Ranked 170/150,000 in the IIT Joint Entrance Examination, India, 1998.	
	Ranked 50/30,000 in the Indian National Physics Olympiad, 1998.	
	Ranked 65/25,000 in the Indian Maths Olympiad, 1997.	
	National Talent Search Exam scholarship, India, 1996. ranked 35/40,000.	
ACADEMIC EXPERIENCE	University of Illinois at Urbana Champaign, Urbana, IL USA	
	<i>Research Assistant, IACOMA Group with Prof. Josep Torrellas</i> Currently working on issues related to processor reliability.	Jan 2003 - present
	<i>Teaching Assistant, CS dept, UIUC</i> Parallel Computer Architecture	spring 2005
	<i>Teaching Assistant, CS dept, UIUC</i> Discrete structures	fall 2002
RESEARCH EXPERIENCE	<i>Selective re-execution of long retired misspeculated instructions using forward slicing</i> fall 2003 Speculation is increasingly assuming an important role in processor design. Nowadays, there are a lot of proposals for speculating on long latency events like reads from memory, dependencies between tasks, remote data from other processors and so on. Upon the detection of a misspeculation, the speculative work is discarded. This is identified as a bottleneck for performance. This work proposes a scheme for selectively re-executing only those instructions that were dependent on the speculated datum. This is referred to as the “forward slice”. But, this is very difficult to do, as such architectures	

speculative retire instructions. Thus, these architectures cannot scan the instructions that are part of the speculative state for dependencies.

This problem was resolved by proposing a theoretical mode for re-execution that can guarantee correctness if four simple conditions are obeyed. These conditions can be easily checked in hardware. This theoretical formalism extends beyond the scope of the paper, and is applicable to any system that employs any kind of a speculation technique (especially speculation of data based on long latency events). An architecture was proposed for such kind of selective re-execution, and it was subsequently evaluated. At the cost of modest hardware complexity, sizable speedups were observed. This work is in the process of submission to MICRO 2005.

Power Analysis of Chip Multiprocessors

spring 2003

This work was performed with Prof. Josep Torrellas. It involved creation of a framework for the measurement of power in our multiprocessor simulator. Later the power and energy consumption of such systems was studied and on the basis of that certain optimizations were proposed.

Characterization of network benchmarks

fall 2002

This was an independent study work performed with Prof. Sarita Adve. Programs from the Net-Bench suite were simulated with RSIM and on the basis of the results certain architectural adaptations were proposed.

Design and simulation of Wan traffic

2001 - 2002

This project involved writing a Wan traffic simulator and studying traffic patterns. The simulator incorporated self-similar models of web traffic. We also worked on a work efficient parallel algorithm for generation of web requests.

Wire cost model of circuits

fall 2001

Verilog code was analyzed and wire cost for certain circuits was modeled.

Design and Implementation of a 4 bit processor

spring 2001

This involved the creation of a 4 bit processor on a bread board. It used a micro- code based control unit. It could support alu, load-store and branch operations.

PUBLICATIONS

Phoenix: Detecting and Recovering from Permanent Processor Design Bugs with Programmable Hardware Smruti R. Sarangi, Abhishek Tiwari and Josep Torrellas. 39th International Symposium on Microarchitecture (MICRO), Dec. 2006.

Designing Hardware that Supports Cycle-Accurate Deterministic Replay Brian Greskamp, Smruti R. Sarangi and Josep Torrellas. Workshop on Complexity Effective Design (along with ISCA 2006)

Rapid Prototyping in Architecture Research using Existing Hardware Mechanisms Smruti R. Sarangi, Brian Greskamp and Josep Torrellas. Workshop on Architectural Research Prototyping (along with ISCA 2006)

Cycle-Accurate Deterministic Replay for Processor Debugging by Smruti R. Sarangi, Brian Greskamp and Josep Torrellas. DSN 2006.

Energy-Efficient Thread-Level Speculation on a CMP by Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti R. Sarangi, James Tuck and Josep Torrellas. IEEE Micro Special Issue: Micro's Top Picks from Computer Architecture, Jan. 2006.

ReSlice: Selective Re-Execution of Long-Retired Misspeculated Instructions Using Forward Slicing by Smruti R. Sarangi, Wei Liu, Josep Torrellas, and Yuanyuan Zhou. 38th International Symposium on Microarchitecture (MICRO), November 2005.

Thread-Level Speculation on a CMP Can Be Energy Efficient by Jose Renau, Karin Strauss, Luis Ceze, Wei Liu, Smruti Sarangi, James Tuck, and Josep Torrellas. 2005 ACM International Conference on Supercomputing (ICS), June 2005.

A Scalable Efficient and General Monte Carlo Scheme for Generating Synthetic Web Request Streams, Smruti R. Sarangi, P.N.Sireesh and S.P.Pal . International Journal of Computer Systems Science and Engineering, Vol. 18, pp, 121-128, May 2003.

OTHER
PROFESSIONAL
EXPERIENCE

Sun Micro-systems, Sunnyvale, CA **May-July 2005**
Worked on the debug architecture of the Rock processor. Designed a novel error detection and recovery technique and looked at other aspects of the DFT architecture. Wrote test benches in Vera to exercise the debug functionalities and evaluated the error coverage.

Summer intern, Niksun Inc., N.J. **May-June 2001**
Worked on a new QOS metric for TCP based applications called TCP Rounds. Niksun later filed a patent application based on this work.

Kent Ridge Digital Labs, Singapore. **May-June 2000**
Java based networking projects using Enterprise Java Beans and Servlets. Wrote an online reward system, auction forum and bulletin board using EJB technologies.

COMPUTER SKILLS

- Prog. Languages : C, C++, Java, Perl, SQL, OCaml, C#, Verilog, Vera
- Technologies : Java Servlets, EJB, XML, .NET
- Operating Systems : Linux, Win 2000/NT, Solaris, FreeBSD Unix
- Software Design : UML, Object Models
- HW platforms : Intel, Dec Alpha, Sun Solaris

GRADUATE LEVEL
COURSES

Parallel algorithms, VLSI, Testing and verification of circuits, Theory of algorithms, Computer Architecture, Programming languages and compilers, Machine learning, Parallel architecture, Advanced Compilers, Advanced Micro-architecture, Automated Deduction, Information Theory, Rapid Prototyping and Evaluation

EXTRA-CURRICULAR
ACTIVITIES

- Treasurer, Indian Graduate Students Association, UIUC, 2004.
- Hawaiian guitar player.
- Member of IEEE and IEEE Computer Society since 2002.