

Pablo Montesinos

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RESEARCH INTERESTS Multicore and parallel computer architecture. Deterministic replay of parallel execution. Programmability of parallel architectures. Architecture support for debugging and program development. Interface between architecture and operating systems.

EDUCATION ○ **University of Illinois at Urbana-Champaign (UIUC)**, Urbana, IL
Ph.D. in Computer Science, June 2009 (expected)
Advisor: Josep Torrellas
Thesis: *Practical Deterministic Replay Of Multiprocessor Systems*
○ **University of Illinois at Urbana-Champaign (UIUC)**, Urbana, IL
M.S. in Computer Science, December 2005
○ **Universidad de León**, Spain
B.S. in Computer Engineering, October 2001

AWARDS AND HONORS ○ **W. J. Poppelbaum Award** - 2009
Awarded by the UIUC Computer Science Department to a graduate student in computer architecture, based on academic merit and creativity.
○ **Selected for a “Research Highlight”** in Communications of the ACM for “*DeLorean: Recording and Deterministically Replaying Shared-Memory Multiprocessor Execution Efficiently*”, 2008
○ **La Caixa Fellowship** - 2003-2005
This program supports the best Spanish graduate students to study abroad.
○ **Valedictorian Award**, Universidad de León - 2001
○ **Education and Science Ministry of Spain**, Research Fellowship - 2000-2001
○ **Department of Mathematics, Universidad de León**, Research Fellowship - 2000
○ **National Champion and European Finalist** - 1997
European Competition for Educational Multimedia Software.
○ **Regional Math Olympics Winner. National finalist** - 1997.

PUBLICATIONS DETERMINISTIC REPLAY AND MULTIPROCESSOR ARCHITECTURE

1. Josep Torrellas, Luis Ceze, James Tuck, Călin Caşcaval, **Pablo Montesinos**, Wonsun Ahn and Milos Prvulovic, ” *The Bulk Multicore Architecture for Improved Programmability* ”. To Appear in Communications of the ACM, December 2009.
2. **Pablo Montesinos**, Matthew Hicks, Samuel T. King and Josep Torrellas, “*Capo: Abstractions and Software-Hardware Interface for Hardware-Assisted Deterministic Multiprocessor Replay*”, 14th International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), March 2009.

3. Derek R. Hower, **Pablo Montesinos**, Luis Ceze, Mark D. Hill and Josep Torrellas, “*Deterministic Replay of Multiprocessor Programs*”, Communications of the ACM (**CACM**), to appear, 2009.
4. **Pablo Montesinos**, Luis Ceze and Josep Torrellas, “*DeLorean: Recording and Deterministically Replaying Shared-Memory Multiprocessor Execution Efficiently*”, 33th Annual International Symposium on Computer Architecture (**ISCA**), Pages: 289-300, June 2008.
5. Luis Ceze, James Tuck, **Pablo Montesinos** and Josep Torrellas, “*Bulk Enforcement of Sequential Consistency*”, 34th Annual International Symposium on Computer Architecture (**ISCA**), Pages: 278-289, June 2007.
6. Luis Ceze, **Pablo Montesinos**, Christoph von Praun, and Josep Torrellas, “*Colorama: Architectural Support for Data-Centric Synchronization*”, 13th International Symposium on High-Performance Computer Architecture (**HPCA**), Pages: 133-144. February 2007

MULTIPROCESSOR PROGRAMMABILITY

7. Luis Ceze, Christoph von Praun, Călin Caşcaval, **Pablo Montesinos**, and Josep Torrellas, “*Programming and Debugging Shared Memory Programs with Data Coloring*”, Workshop on Compilers for Parallel Computing (**CPC**), January 2009
8. Luis Ceze, Christoph von Praun, Călin Caşcaval, **Pablo Montesinos**, and Josep Torrellas, “*Concurrency Control with Data Coloring*”, Workshop on Memory Systems Performance and Correctness (**MSPC**), March 2008

PROCESSOR AND SYSTEM RELIABILITY

9. **Pablo Montesinos**, Wei Liu, and Josep Torrellas, “*Using Register Lifetime Predictions To Protect Register Files Against Soft Errors*”, Extended version of [10]. Invited Paper to the IEEE Transactions on Dependable and Secure Computing, (**IEEE TDSC**), to appear, 2009
10. **Pablo Montesinos**, Wei Liu, and Josep Torrellas, “*Using Register Lifetime Predictions to Protect Register Files Against Soft Errors*”, 37th International Conference on Dependable System and Networks (**DSN**). Pages 286-296. June 2007
11. **Pablo Montesinos**, Wei Liu, and Josep Torrellas, “*Shield: Cost-Effective Soft-Error Protection for Register Files*”, Third IBM TJ Watson Conference on Interaction between Architecture, Circuits and Compilers (**PAC²**), October 2006
12. Jun Nakano, **Pablo Montesinos**, Kourosh Gharachorloo, and Josep Torrellas, “*ReViveI/O: Efficient Handling of I/O in Highly-Available Rollback-Recovery Servers*”, 12th International Symposium on High-Performance Computer Architecture (**HPCA**), Pages: 203-214. February 2006

OTHER PAPERS AND SOFTWARE

13. **Pablo Montesinos**, “*Stage Driver*”, 12th Conference on Pattern Languages of Programs (**PLoP**). June 2005
14. Jose Renau, Basilio Fraguera, James Tuck, Wei Liu, Milos Prvulovic, Luis Ceze, Smruti Sarangi, Paul Sack, Karin Strauss and **Pablo Montesinos**. “*SESC Simulator*”, <http://sesc.sourceforge.net>. 2005

PAPERS UNDER REVIEW

15. **Pablo Montesinos**, Matthew D. Hicks, Wonsun Ahn, Samuel T. King and Josep Torrellas, " *Lessons Learned During the Development of the CapoOne Deterministic Multiprocessor Replay System*". Submitted for publication. 2009.

THESES

- Master Thesis: "*Shield: Resource-Efficient Protection for Register Files*", UIUC. May 2005. Advisor: Josep Torrellas
- B.S. Diploma Thesis: "*Compressed File Systems*", Universidad de León. September 2001. Advisor: Araceli de Francisco

RESEARCH

- **Graduate Research Assistant**, i-acoma group, UIUC.

EXPERIENCE

2003-present.

Advisor: Josep Torrellas.

I work in the Intel-Microsoft Universal Parallel Computer Research Center (UPCRC) at the University of Illinois. My research has focused on hardware and software support for multiprocessor architectures. A major emphasis has been effective deterministic replay of multicore systems. Specifically, I proposed *Capo* (ASPLOS'09), the first software-hardware interface for practical hardware-assisted deterministic replay of shared-memory multiprocessors, and developed *CapoOne*, its first implementation. High-performance multiprocessor replay needs a system that can efficiently record the interleaving of memory operations. Thus, I proposed and evaluated *DeLorean* (ISCA'08, CACM'09), a new hardware architecture for high-speed deterministic replay based on chunk execution (ISCA'07).

Another area I have worked on is improving the programmability of multiprocessors, including a novel architecture (HPCA'07) and programming models for hardware-based data centric synchronization (CPC'09, MSPC'08, HPCA'07).

Finally, I have also worked on reliability, at both processor and system level. At the processor level, I proposed *Shield* (IEEE TDSC'09 ,DSN'07, PAC²'06), an efficient register-file protection mechanism where registers are only protected while they contain useful data. At the system level, I have helped implement and evaluate *ReVive I/O*, a scheme that enables I/O undo/redo in architectures with high-frequency checkpointing (HPCA'06).

- **Graduate Research Intern**, Intel Corporation. Oregon.

Summer 2006.

Mentor: Scott Hahn.

I evaluated and optimized virtualization environments for manycore architectures.

- **Research Intern**, Universidad de León.

2000-2001

Advisor: Araceli de Francisco Iribarren.

I developed and evaluated a kernel driver for the BeOS operating system that was able to read, write and mount compressed volumes.

TEACHING

- **Teaching Assistant**, *Parallel Computer Architectures*. UIUC.

EXPERIENCE

Spring 2006 and Spring 2008.

Advanced graduate-level course with 30 students. Topics included research issues in parallel architectures. Responsibilities included assigning and grading homeworks and class projects, as well as holding office hours. I also gave multiple lectures.

- **Lecturer**, *Introduction to Operating Systems*. Universidad de León. February 2003 - August 2003.
Undergraduate level course with 100 students. Topics included basic concepts on operating systems. Responsibilities included lecturing two times per week, assigning and grading homeworks, machine problems and exams, as well as holding office hours.

- **Lecturer**, *Operating System Design*. Universidad de León. February 2003 - August 2003.
Undergraduate level course with 15 students. Topics included operating systems architecture. Responsibilities included lecturing two times per week, assigning and grading homeworks, machine problems and exams, as well as holding office hours.

TALKS

- *Capo: Abstractions and Software-Hardware Interface for Hardware-Assisted Deterministic Multiprocessor Replay*, 14th International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**), March 2009.
- *Efficient Recording and Deterministic Replay of Shared-Memory Multiprocessor Programs*. Intel-Microsoft Universal Parallel Computing Research Center at the University of Illinois. December 2008.
- *Efficient Recording and Deterministic Replay of Shared-Memory Multiprocessors*. Intel Corp. Hillsboro, Oregon. October 2008.
- *Recording and Deterministically Replaying Shared Memory Multiprocessor Execution Efficiently*, 35th Annual International Symposium on Computer Architecture (**ISCA**), Beijing, China, June 2008.
- *Chunk-Based Execution and Deterministic Replay*. Invited talk. Guest speaker at the Departamento de Ingeniería Eléctrica y Electrónica, Universidad de León. Spain, May 2008.
- *Concurrency Control with Data Coloring*, Workshop on Memory Systems Performance and Correctness, Seattle, March 2008
- *Using Register Lifetime Predictions to Protect Register Files Against Soft Errors*, 37th International Conference on Dependable System and Networks (**DSN**), Edinburgh, Scotland. June 2007.
- *Shield: Cost-Effective Soft-Error Protection for Register Files*, Third IBM TJ Watson Conference on Interaction between Architecture (**PAC²**), Yorktown Heights, NY. October 2006.
- *ReViveI/O: Efficient Handling of I/O in Highly-Available Rollback-Recover y Servers*, 12th International Symposium on High-Performance Computer Architecture (**HPCA**), Austin, Texas. February 2006.

INDUSTRY
EXPERIENCE

- **Junior R&D Developer**, Ydilo Advanced Voice Solutions. Madrid, Spain. June 2002 - December 2002. Design and development of voice applications based on Java, C++, Oracle and NUANCE systems.

SERVICE

- Organized seminar in UIUC research group (2006-2007).
- Reviewer for ASPLOS, DSN, HPCA, ISCA, MICRO, IEEE Transactions on Computers.
- Student Member of IEEE and ACM.
- President and Secretary of *Unicyber*, a student organization at the Universidad de León.

- REFERENCES
- **Prof. Josep Torrellas.**
Advisor, Dissertation chair.
Department of Computer Science, UIUC.
torrellas@cs.uiuc.edu

 - **Prof. Samuel T. King.**
Co-Advisor. Dissertation committee member.
Department of Computer Science, UIUC.
kingst@cs.uiuc.edu

 - **Prof. Marc Snir.**
Dissertation committee member.
Department of Computer Science, UIUC.
snir@cs.uiuc.edu

 - **Prof. Wen-mei W. Hwu.**
Dissertation committee member.
Electrical and Computer Engineering, UIUC.
hwu@crhc.uiuc.edu

 - **Prof. Yuanyuan Zhou.**
Dissertation committee member.
Department of Computer Science, UIUC.
yyzhou@cs.uiuc.edu

 - **Prof. Christoph von Praun.**
Dissertation committee member.
Georg-Simon-Ohm University, Department of Computer Science. Nuremberg, Germany.
praun@acm.org

 - **Scott Hahn.**
Intel Mentor.
Intel Labs, Hillsboro, Oregon.
scott.hahn@intel.com