

# ABDULLAH MUZAHID

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## Research Interests

Parallel computer architecture, programmability of parallel systems, concurrency bug detection and avoidance, parallel programming models.

## Education

- August 2006 to Present, PhD Student, Department of Computer Science, University of Illinois at Urbana-Champaign (UIUC)
  - GPA: 3.95/4.00
  - Expected graduation date: June 2012
  - Thesis: *Effective architectural support for debugging concurrency bugs*
  - Advisor: Prof. Josep Torrellas
- May 2009, Master of Science, Department of Computer Science, UIUC
  - GPA: 3.95/4.00
  - Thesis: *Data Race Detection Using Signatures*
  - Advisor: Prof. Josep Torrellas
- May 2005, Bachelor of Science, Department of Computer Science and Engineering, Bangladesh University of Engineering & Technology (BUET)
  - GPA: 3.99/4.00 (**1st** in the whole university)

## Honors

- **Intel PhD Fellowship, 2011**
- **Mavis Future Faculty Fellowship, UIUC, 2011**
- Nominated for Intel PhD Fellowship by UIUC, 2010
- MICRO Conference Travel Grant, 2010
- ISCA Conference Travel Grant, 2009
- Abbasi Fellowship, UIUC, 2006
- University Fellowship, Ohio State University, 2006 (declined)
- Prime Minister Gold Medal for securing the 1st position in the School of Electrical and Electronics Engineering, BUET, 2006
- University Gold Medal, BUET, 2006
- Sharfuddin Gold Medal, Department of Computer Science and Engineering, BUET, 2006

## Publications

- **Conference Papers:**

- **Abdullah Muzahid**, Shanxiang Qi, and Josep Torrellas. Vulcan: Architectural Support for Dynamically Detecting Sequential Consistency Violations in Programs. *Submitted for publication*.
- Shanxiang Qi, **Abdullah Muzahid**, and Josep Torrellas. Swift: Dynamically Detecting and Tolerating IF-condition Data Races. *Submitted for publication*.
- Shanxiang Qi, Norimasa Otsuki, Lois Nogueira, **Abdullah Muzahid**, and Josep Torrellas. AsymRace: Tolerating Asymmetric Data Races with Unintrusive Hardware. In *International Symposium on High Performance Computer Architecture (HPCA)*, February 2012.
- **Abdullah Muzahid**, Norimasa Otsuki, and Josep Torrellas. AtomTracker: A Comprehensive Approach to Atomic Region Inference and Violation Detection. In *International Symposium on Microarchitecture (MICRO)*, December 2010.
- **Abdullah Muzahid**, Dario Suarez, Shanxiang Qi, and Josep Torrellas. SigRace: Signature-Based Data Race Detection. In *International Symposium on Computer Architecture (ISCA)*, June 2009.
- **Abdullah Muzahid**, Ahmed Khurshid, Md. Mostofa Akbar, and Masud Karim Khan. Reservation Based Adaptive Uplink Admission Control for WCDMA. In *International Conference on Next Generation Wireless Systems (ICNEWS)*, January 2006.

- **Posters:**

- **Abdullah Muzahid**, Dario Suarez, Shanxiang Qi, and Josep Torrellas. Architectural Support for Detecting Data Races and Atomicity Violations. In *Intel Developer Forum (IDF)*, September 2009.
- **Abdullah Muzahid**, and Le-Chun Wu. Performance Evaluation of Dynamic Thread Balancing in Google's Threading Library. In *Google Summer Intern Project Poster Show*, August 2008.

- **Master's Thesis:**

*Data Race Detection Using Signatures*

Advisor: Prof. Josep Torrellas

Department of Computer Science, UIUC, May 2009

- **Undergraduate Thesis:**

*Reservation Based Adaptive Uplink Admission Control for WCDMA*

Advisor: Prof. Md. Mostofa Akbar

Department of Computer Science and Engineering, BUET, May 2005

## Presentations

- "Vulcan: Architectural Support for Dynamically Detecting Sequential Consistency Violations in Programs". At Intel Corporation, Champaign, IL, November 2011.
- "AtomTracker: A Comprehensive Approach to Atomic Region Inference and Violation Detection". At Universal Parallel Computing Research Center, UIUC, February 2011.

- “AtomTracker: A Comprehensive Approach to Atomic Region Inference and Violation Detection”. At International Symposium on Microarchitecture (MICRO), December 2010.
- “AtomTracker: A Comprehensive Approach to Atomic Region Inference and Violation Detection”. At Intel Corporation, Champaign, IL, October 2010.
- “Effectiveness of Sharing Analysis in Intel Thread Checker”. At Intel Corporation, Champaign, IL, August 2010.
- “SigRace: Signature-Based Data Race Detection”. At Universal Parallel Computing Research Center, UIUC, May 2009.
- “SigRace: Signature-Based Data Race Detection”. At International Symposium on Computer Architecture (ISCA), June 2009.
- “Performance Evaluation of Dynamic Thread Balancing in Google’s Threading Library”. At Google, Mountain View, CA, August 2008.
- “Reservation Based Adaptive Uplink Admission Control for WCDMA”. At International Conference on Next Generation Wireless Systems (ICNEWS), January 2006.

## Professional Experience

- August 2007 to Present, Research Assistant, UIUC
  - Working in the I-ACOMA Research Group
  - Advisor: Prof. Josep Torrellas
- May 2010 to August 2010, Intern, Intel Corporation
  - Worked in Intel’s Thread Checker group
  - Mentors: Xiurong Zhu and Matthew Frank
- May 2008 to August 2008, Intern, Google
  - Worked in Google’s Multicore Software group
  - Mentor: Le-Chun Wu
- January 2009 to May 2009 and January 2012 to May 2012, Teaching Assistant, UIUC
  - Course: Parallel Computer Architectures (CS 533)
  - Instructor: Prof. Josep Torrellas
- June 2005 to July 2006, Lecturer, Department of Computer Science and Engineering, BUET
  - Course: Microprocessors and Digital Computers (CSE 421)
  - Lab classes: Data structures, artificial intelligence, microprocessor design, operating systems, networking and database design
- November 2005 to July 2006, Consultant, Ministry of Planning, Government of Bangladesh
  - Conducted full survey of the secretariat buildings
  - Designed network infrastructure and e-governance project

## Research Experience

- **Sequential Consistency Violation Detection**, January 2011 to Present  
*UIUC, under Prof. Josep Torrellas*

Sequential consistency (SC) is the most intuitive memory model for multiprocessors. However, it is very restrictive and disallows many access re-orderings. This is why, modern processors employ some form of relaxed memory model. However, these machines can easily lead to SC violations, which are almost always bugs. In this work, we detect SC violations at runtime with novel architectural support. In the course of doing so, we also discover three new bugs in popular codes. This work is currently submitted for publication.

- **If-Condition Data Race Detection**, June 2011 to Present  
*UIUC, under Prof. Josep Torrellas*

Our study on the characteristics of real world data races has shown that many data races occur in the if-then-else constructs. Specifically, programmers usually assume that variables used in the if-condition remain unchanged during the execution of the whole if construct. However, because of data races, sometimes the condition gets changed by a remote processor before the construct is finished. This typically leads to incorrect results or even crashes. In this work, we detect if-condition data races very cheaply in software and also in hardware. The hardware, in addition to detecting the bug, can avoid it too. This work is currently submitted for publication.

- **Atomicity Violation Detection**, January 2009 to December 2010  
*UIUC, under Prof. Josep Torrellas*

Atomicity violation is a type of concurrency bug where a sequence of supposedly atomic instructions is unserializably interleaved with instructions from other threads that access the same memory locations. To identify and eliminate these bugs, we propose a novel architectural design. Our proposal is unique in that it is the first one to handle *general* atomic regions — i.e., regions not limited by instruction count, variable count or code construct. Our proposal identifies possible atomic regions in the code by analyzing several training runs, and then detects violations of these regions very efficiently with architectural support. We have recently published a paper on this in the International Symposium on Microarchitecture (MICRO) in December 2010.

- **Asymmetric Data Race Detection and Tolerance**, May 2009 to May 2011  
*UIUC, under Prof. Josep Torrellas*

A type of data race that has not received much attention is Asymmetric data races. In this case, the state of a well tested and correct thread executing a critical section is corrupted by a buggy, racing thread. This type of race is particularly prominent when interfacing with the third party code like the driver code in the OS. Existing approaches use software techniques and, therefore, incur huge execution overhead. Besides, they introduce problems like deadlocks. We propose to detect and tolerate asymmetric data races with the help of address signatures. Our scheme has low execution overhead and does not induce deadlocks. We published a paper on this in the International Symposium on High Performance Computer Architecture (HPCA) in February 2012.

- **Sharing Analysis of Intel Thread Checker**, May 2010 to August 2010  
*Intel Corporation, under Xiurong Zhu and Matthew Frank*

We perform a detailed study of the benefits of data sharing detection in Intel's Thread Checker. The idea is to determine which instructions of a program may access shared data, and then in the later race-detection phase, instrument only those instructions. This approach reduces the execution time of the race-detection phase by around 50%. We also propose some other low-overhead optimizations like redundant call and return elimination, and redundant stack processing.

- **Data Race Detection**, January 2008 to May 2009  
*UIUC, under Prof. Josep Torrellas*

We propose novel architectural support for detecting data races with low overhead and high coverage. All previous hardware-based data race detectors tag cache lines with extra bits and piggyback information on cache-coherence protocol messages. Such an approach complicates key hardware structures and is not effective when a line gets displaced or invalidated from the cache. In this work, we propose using hardware address signatures to capture the memory access history. These signatures are periodically sent to an on-chip module which compares signatures from different cores to find out possible data races. We published a paper on this in the International Symposium on Computer Architecture (ISCA) in June 2009.

- **Performance Benchmarking of Threading Primitives**, May 2008 to August 2008  
*Google, under Le-Chun Wu*

We benchmark and load-test various threading primitives developed by Google. We develop a framework to measure the performance of the thread creation library. We benchmark a threading primitive that dynamically creates and destroys active threads to maximize system utilization. This work is now a part of the permanent code base of Google.

- **Data Centric Synchronization**, June 2007 to December 2007  
*UIUC, under Prof. Josep Torrellas*

We study architectural support for implementing data centric synchronization (DCS). In DCS, the programmer associates synchronization constraints to data structures (e.g., which data structures need to be accessed together in the same critical section). Whenever any of these data is accessed, the hardware automatically starts a critical section and prevents other threads from accessing the data structures. DCS significantly simplifies parallel programming.

- **Study of Uplink Admission Control for WCDMA**, March 2004 to April 2005  
*BUET, under Prof. Mostofa Akbar*

We study various strategies of Admission Control (AC) in WCDMA (3G Wireless Systems). We also propose a new AC algorithm that (i) has provision for multiple service classes with varying data rates, (ii) establishes certain levels of QoS, (iii) auto-tunes the maximum tolerable system interference threshold, and (iv) pre-reserves system resources for users based on their system usage profile. We published a paper on this in the International Conference on Next Generation Wireless Systems (ICNEWS) in January 2006.

## Teaching Experience

- **Teaching Assistant**, January 2009 to May 2009 & January 2012 to May 2012, UIUC

I worked as a teaching assistant for the advanced graduate level course “Parallel Computer Architectures (CS 533)”. Besides preparing homeworks and grading them, I taught several lectures. I tried to connect my research with what I taught. I taught classes on synchronization, reliability, and OS/hardware interactions. I incorporated relevant papers from recent top conferences to keep the students updated about the ongoing research issues.

- **Lecturer**, June 2005 to July 2006, Department of Computer Science and Engineering, BUET

I was the instructor of the course “Microprocessors and Digital Computers (CSE 421)” at the senior level. I designed the course curriculum, homeworks and project ideas. I also prepared the final’s questions. To provide the students’ some hands-on experience about microprocessor design, I developed a lab project where they had to implement a simple 4-bit processor capable of executing a recursive program. I also provided several project ideas where the students had to use 8080/8086 microprocessors to design some simple devices like a stop watch, a traffic light system, a taxi cab meter etc. In addition to this full course, I organized lab classes on data structures, artificial intelligence, operating systems, networking and database design.

## Technical Skills

- Operating Systems: Linux, Unix, Windows 98/2000/XP/Vista/7, OS X
- Programming Languages: C, C++, Java
- Scripting Languages: Bash, Python
- Binary Instrumentation Tool: PIN
- Compiler Framework: LLVM
- Simulator: SESC, Simics, FeS2

## Services & Extracurricular Activities

- External reviewer for the HPCA, ASPLOS, MICRO and ISCA conferences
- Member of the Dean’s Graduate Student Advisory Committee, UIUC, August 2009 to July 2010
- Organizer of the seminars of the I-ACOMA research group, January 2009 to December 2009
- Involved with the graduate student mentoring program, August 2008 to July 2009
- Organizer of the project shows of CSE Day’06 in BUET

## Status

Citizen of Bangladesh, holding F-1 visa.

## References

- **Josep Torrellas** (advisor)  
Professor, Department of Computer Science  
University of Illinois at Urbana-Champaign  
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- **Marc Snir**  
Professor, Department of Computer Science  
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