

Brian Greskamp — Curriculum Vitæ

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RESEARCH INTERESTS Multicore and parallel computer architecture. Single-thread performance in multicores. Better-than-worst-case design. Technology-driven architectures. Variation-aware architectures. Interaction of architecture, power, and reliability.

EDUCATION ◦ **University of Illinois at Urbana-Champaign** (UIUC), Urbana, IL
Ph.D. in Computer Science, July 2009
Advisor: Josep Torrellas
Thesis: *Enhancing Single-Thread Performance in Chip Multiprocessors with Timing Speculation*

◦ **Clemson University**, Clemson, SC
B.S. in Computer Engineering, August 2003
4.0 GPA, *Summa cum laude*
Advisor: Prof. Ron Sass
Thesis: *A Java Virtual Machine for Runtime Reconfigurable Computing*

PUBLICATIONS MULTICORE AND PROCESSOR ARCHITECTURE

1. R. Ulya Karpuzcu, **Brian Greskamp**, and Josep Torrellas, “*The BubbleWrap Many-core: Popping Cores for Sequential Acceleration*”, International Symposium on Microarchitecture (**MICRO**), December 2009.
2. **Brian Greskamp**, Lu Wan, Ulya R. Karpuzcu, Jeffrey J. Cook, Josep Torrellas, Deming Chen, and Craig Zilles, “*BlueShift: Designing Processors for Timing Speculation from the Ground Up*”, International Conference on High-Performance Computer Architecture (**HPCA**), February 2009.
3. **Brian Greskamp** and Josep Torrellas, “*Paceline: Improving Single-Thread Performance in Nanoscale CMPs through Core Overclocking*”, International Conference on Parallel Architecture and Compilation Techniques (**PACT**), September 2007.
4. **Brian Greskamp** and Josep Torrellas, “*Composing Low Overhead Voltage and Frequency Techniques for Single Thread Performance in Configurable Multicores*”, **under submission**.
5. **Brian Greskamp**, Ulya R. Karpuzcu, and Josep Torrellas, Short paper: “*BubbleWrap: Popping CMP Cores for Per-Thread Performance*”, Wild and Crazy Ideas Session at ASPLOS (**WACI**), March 2009.

VARIATION-AWARE MICROARCHITECTURE

6. Smruti R. Sarangi, **Brian Greskamp**, Abhishek Tiwari, and Josep Torrellas, “*EVAL: Utilizing Processors with Variation-Induced Timing Errors*”, International Symposium on Microarchitecture (**MICRO**), November 2008.
7. Smruti R. Sarangi, **Brian Greskamp**, Radu Teodorescu, Jun Nakano, Abhishek Tiwari and Josep Torrellas “*VARIUS: A Model of Process Variation and Resulting Timing Errors for Microarchitects*”, IEEE Transactions on Semiconductor Manufacturing (**IEEE TSM**), February 2008.
8. **Brian Greskamp**, Smruti R. Sarangi, and Josep Torrellas, “*Threshold Voltage Variation Effects on Aging-Related Hard Failure Rates*”, International Symposium on Circuits and Systems (**ISCAS**), Special Session: Circuit Design in the Presence of Device Variability, May 2007.
9. Smruti R. Sarangi, **Brian Greskamp**, and Josep Torrellas, “*A Model for Timing Errors in Processors with Parameter Variation*”, International Symposium on Quality Electronic Design (**ISQED**), March 2007.
10. Radu Teodorescu, **Brian Greskamp**, Jun Nakano, Smruti R. Sarangi, Abhishek Tiwari and Josep Torrellas, “*VARIUS: A Model of Parameter Variation and Resulting Timing Errors for Microarchitects*”, Workshop on Architectural Support for Gigascale Integration (**ASGI**), June 2007. This is an early version of [7].

RELIABILITY AND COMPLEXITY

11. Cyrus Bazeghi, Francisco J. Mesa-Martínez, **Brian Greskamp**, Josep Torrellas, and José Renau. “*Estimating Design Time for System Circuits*”, Conference on Very Large Scale Integration Systems on Chip (**VLSI-SoC**), October 2007.
12. **Brian Greskamp**, Smruti R. Sarangi, and Josep Torrellas, “*Designing Hardware that Supports Cycle-Accurate Deterministic Replay*”, Workshop on Complexity-Effective Design (**WCED**), June 2006.
13. Smruti R. Sarangi, **Brian Greskamp**, and Josep Torrellas, “*CADRE: Cycle-Accurate Deterministic Replay for Hardware Debugging*”, International Conference on Dependable Systems and Networks (**DSN**), June 2006.
14. Smruti R. Sarangi, **Brian Greskamp**, and Josep Torrellas, “*Rapid Prototyping in Architecture Research using Hardware Hooks in COTS Systems*”, Workshop on Architecture Research Prototyping (**WARP**), June 2006.
15. Cyrus Bazeghi, Francisco J. Mesa-Martínez, **Brian Greskamp**, Josep Torrellas, and José Renau. “*μComplexity: Estimating Processor Design Effort*”, University of Illinois Technical Report UIUCDCS-R-2005-2644, August 2005.

RECONFIGURABLE COMPUTING

16. Ron Sass, **Brian Greskamp**, Brian Leonard, Jeff Young, and Sreenivas Beeravolu “*Online Architectures: A Theoretical Formulation and Experimental Prototype*”, Journal of Microprocessors and Microsystems (**JMM**), September 2006.

17. **Brian Greskamp** and Ron Sass, Short paper: “*A Virtual Machine for Merit-Based Runtime Reconfiguration*”, Conference on Field Programmable Custom Computing Machines (FCCM), April 2005.

RESEARCH ○ **Hardware Design Engineer**

EXPERIENCE D. E. Shaw Research, (2009 – present)

Design specialized hardware for biomolecular simulation.

○ **Graduate Research Assistant**

i-acoma group, UIUC (2004 – 2009)

Advisor: Prof. Josep Torrellas.

Timing Speculation (2007 – present): Explored techniques to enhance single-thread performance on Chip Multiprocessors (CMPs). Developed the Paceline architecture for low-overhead, configurable timing speculation on CMPs [3]. Collaborated with Prof. Deming Chen to develop the BlueShift [2] design flow, which enhances performance on timing speculation architectures like Paceline. Composed timing speculation and voltage scaling to speed up cores in a lightly-loaded CMP [4].

Process Variation (2006 – 2008): Contributed to the development of the VARIUS process variation model [7, 9] and characterized the effects of variation on timing errors and circuit aging [8]. Additionally, I worked on EVAL, an architecture designed specifically to tolerate variation-induced timing errors [6].

Design Complexity (2004 – 2006): Collaborated with Prof. Jose Renau to develop predictive metrics for processor design effort. The work produced a new metric, μ Complexity, that correlates structural metrics from the RTL implementation with total logic design and verification effort (in person months) [11, 15]. I also worked on developing fully deterministic system architectures to ease hardware bringup and debugging [12, 13, 14].

○ **Graduate Research Intern**

Sun Microsystems (Summer 2007)

Mentor: John Fredrickson

Evaluated trace-based simulation methods for predicting the performance of many-core CMPs.

○ **Graduate Research Intern**

General Electric Global Research (Summer 2004)

Mentor: Austars Schnore

Evaluated HPC platforms for in-house numerical codes and wrote an *eclipse* development environment for FPGA-based signal-processing.○ **Graduate Research Assistant**

ECE Dept., University of Illinois (Fall 2003 – Spring 2004)

Advisor: Prof. Nick Carter

Developed compiler infrastructure for the Amalgam architecture, which contains both CPU and FPGA-based processing elements.

○ **Undergraduate Researcher**

ECE Dept., Clemson University (Fall 2002 – Spring 2003)

Advisor: Prof. Ron Sass

Developed extensions to the Java Virtual Machine to manage the runtime partitioning of a Java application's kernels between a host CPU and an FPGA-based compute accelerator [16, 17].

- **Undergraduate Intern**
ADTRAN Inc. (Three semesters during 2001 — 2002)
Integrated OSPF IP routing protocol into *Netvanta* edge router. Developed, maintained, and tested network card firmware. Performed security testing for router and firewall products.
- TEACHING EXPERIENCE ○ **Teaching Assistant**
CS Dept., University of Illinois (Spring 2006, Spring 2008)
Part-time TA for ECE/CS 533: Parallel Computer Architecture. Prepared two major homeworks, held office hours for students, delivered miscellaneous lectures.
- **Robot League Mentor**
Champaign, IL school district (Fall 2006)
FIRST Lego Robotics League mentor for grades 5 and 6. Acted as facilitator while kids researched nanotech fabrication techniques and designed Lego Mindstorm robots.
- **Teaching Assistant**
ECE Dept., University of Illinois (Fall 2003 – Spring 2004)
Taught laboratory sections for ECE 385: Digital Systems Laboratory. Received **top 5% TA rating**.
- TALKS ○ *BlueShift: Designing Processors for Timing Speculation from the Ground Up*, International Conference on High-Performance Computer Architecture, February 2009.
- *EVAL: Utilizing Processors with Variation-Induced Timing Errors*, International Symposium on Microarchitecture, November 2008.
- *Paceline: Improving Single-Thread Performance in Nanoscale CMPs through Core Overclocking*, International Conference on Parallel Architectures and Compilation Techniques, September 2007.
- *A Model of Parameter Variation and Resulting Timing Errors for Microarchitects*, Workshop on Architectures for Gigascale Integration, June 2007.
- *A Model for Timing Errors in Processors with Parameter Variation*, International Symposium on Quality Electronic Design, March 2007.
- *Threshold Voltage Variation Effects on Aging-Related Hard Failure Rates*, International Symposium on Circuits and Systems, May 2007.
- *Designing Hardware that Supports Cycle-Accurate Deterministic Replay*, Workshop on Complexity-Effective Design, June 2006.
- *A Virtual Machine for Merit-Based Runtime Reconfiguration*, Conference of Field Programmable Custom Computing Machines, April 2005.
- SERVICE Reviewer for ASPLOS, DSN, HPCA, ISCA, MICRO.
Student Member of IEEE.
- REFERENCES ○ **Prof. Josep Torrellas**. Department of Computer Science, UIUC
Advisor, dissertation chair.
torrellas@cs.uiuc.edu
- **Prof. Deming Chen**. Department of ECE, UIUC
Co-advisor, dissertation committee member.
dchen@illinois.edu

- **Prof. Sanjay Patel.** Department of ECE, UIUC
Dissertation committee member.
sjp@illinois.edu
- **Prof. Craig Zilles.** Department of Computer Science, UIUC
Dissertation committee member.
zilles@illinois.edu
- **Shekhar Y. Borkar.** Director, Intel Microprocessor Technology Lab
Dissertation committee member.
shekhar.y.borkar@intel.com