

Abhishek Tiwari

CONTACT INFORMATION

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RESEARCH INTERESTS

Computer architecture, Multicore architecture, Reliability, Technology scaling issues, Process variation, Aging, Design defects, Machine learning, Data integration

EDUCATION

University of Illinois at Urbana-Champaign, Urbana, Illinois USA

Ph.D., Computer Science, August 2008, expected

- Advisor: Prof. Josep Torrellas
- Thesis title: Hiding and Mitigating the Impact of Spatial and Temporal Variation on Processor Performance and Power
- GPA: 4.0/4.0

M.S., Computer Science, May 2005

- Advisor: Prof. AnHai Doan
- Thesis title: Profile Based Object Matching for Data Integration
- GPA: 4.0/4.0

Indian Institute of Technology, Kanpur, India

B.Tech., Computer Science and Engineering, May 2003

- GPA: 9.9/10.0(3.96/4.0)

AWARDS AND HONORS

2006 Paper in IEEE Micro Magazine, Special Issue “2006 Micro’s **Top Picks** from Computer Architecture Conferences”

2006 **Best Paper Award**, 39th International Symposium on Microarchitecture (MICRO), December 2006

2003–2006 ILLIAC Fellowship, University of Illinois at Urbana-Champaign, awarded to outstanding graduate students in computer science. The award is named after the historic ILLIAC projects at UIUC.

2003 Ratan Swarup Memorial Prize, IIT Kanpur, for excellent all-round performance in the graduating class

2001 Winner, ACM International Collegiate Programming Contest, Asia

1999 Aditya Birla Scholarship, IIT Kanpur, awarded to top 10 students from all Indian Institutes of Technology (IIT), for outstanding academic excellence and humane leadership values

1999 All India Rank 12 in Indian Institute of Technology, Joint Entrance Exam (IIT-JEE)

1997 National Talent Search Scholarship (NTSE), awarded to 750 most brilliant high school students in India

PUBLICATIONS

Smruti R. Sarangi, Brian Greskamp, Radu Teodorescu, Jun Nakano, **Abhishek Tiwari**, and Josep Torrellas. VARIUS: A Model of Process Variation and Resulting Timing Errors for Microarchitects. *IEEE Transactions on Semiconductor Manufacturing (IEEE TSM)*, February 2008. (25 pages)

Radu Teodorescu, Jun Nakano, **Abhishek Tiwari**, and Josep Torrellas. Mitigating Parameter Variation with Dynamic Fine-Grain Body Biasing. 40th *International Symposium on Microarchitecture (MICRO)*, December 2007. (12 pages, 20% acceptance rate)

Abhishek Tiwari, Smruti R. Sarangi, and Josep Torrellas. ReCycle: Pipeline Adaptation to Tolerate Process Variation. *34th International Symposium on Computer Architecture (ISCA)*, June 2007. (12 pages, 23% acceptance rate, 46/204)

Radu Teodorescu, Brian Greskamp, Jun Nakano, Smruti R. Sarangi, **Abhishek Tiwari**, and Josep Torrellas. VARIUS: A Model of Parameter Variation and Resulting Timing Errors for Microarchitects. *Workshop on Architectural Support for Gigascale Integration (ASGI), in conjunction with ISCA*, June 2007. (9 pages)

Smruti R. Sarangi, **Abhishek Tiwari**, and Josep Torrellas. Phoenix: Detecting and Recovering from Permanent Processor Design Bugs with Programmable Hardware. *39th International Symposium on Microarchitecture (MICRO)*, December 2006. **Best Paper Award**. (12 pages, 24% acceptance rate, 42/174)

Smruti R. Sarangi, Satish Narayanasamy, Bruce Carneal, **Abhishek Tiwari**, Brad Calder, and Josep Torrellas. Patching Processor Design Errors with Programmable Hardware. *IEEE Micro Magazine Special Issue: 2006 Micro's Top Picks from Computer Architecture Conferences*, January-February 2007. (14 pages, 14% acceptance rate, 11/76)

SUBMITTED FOR
PUBLICATION

Abhishek Tiwari and Josep Torrellas. Facelift: Hiding and Slowing Down Aging in Multicores. November 2007, submitted for publication to a conference.

THESES

Profile Based Object Matching for Data Integration. Masters Thesis, Advised by Prof. AnHai Doan, UIUC, May 2005.

ACADEMIC
EXPERIENCE

University of Illinois at Urbana-Champaign, Urbana, Illinois USA

Research Assistant

January 2005 - present

Developed a model for processor aging (wearout). Implemented in software and evaluated techniques to mitigate the effects of variation and aging on power and performance. Worked on a framework for recovering from processor design bugs. Involved programming in the R statistical language.

- Supervisor: Prof. Josep Torrellas

Research Assistant

May 2004 - December 2004

Proposed and implemented a machine learning algorithm for object matching to support data integration. Required advanced skills in Perl scripting.

- Supervisor: Prof. AnHai Doan

TEACHING
EXPERIENCE

Teaching Assistant

- Course: Parallel Computer Architecture (CS533) *Spring 2006*
- Advanced graduate course, with about 30 students

INTERNSHIPS

Applications Research Lab (ARL), Intel Research, Santa Clara **May 2006 - August 2006**

Researched and developed architectural features to manage resources on multi-core systems to improve application scalability. Worked on next generation recognition, mining and synthesis (RMS) applications as outlined by Pat Gelsinger's keynotes. Involved C/C++ programming on an industrial strength microarchitecture simulator in a UNIX/Linux environment.

- Supervisors: Dr. Christopher J. Hughes and Dr. Sanjeev Kumar

Max Planck Institut für Informatik, Saarbrücken, Germany

May 2002 - July 2002

Developed and implemented an efficient algorithm for hidden surface removal from terrains. Involved C++ programming with STL. Worked in the Algorithms and Computational Geometry group (AG1).

- Supervisors: Dr. Lutz Kettner and Dr. Susan Hert

Tata Institute for Fundamental Research, Pune, India **May 2001 - July 2001**

Worked with Prof. Narendra Karmarkar to apply the Karmarkar's algorithm for linear programming to solve NP-hard problems. Prof. Karmarkar was awarded the Paris Kanellakis award in 2000 for devising a polynomial time algorithm for linear programming.

TALKS

“ReCycle: Adaptive Pipelining for Tolerating Process Variation.” Conference Talk at the International Symposium on Computer Architecture (ISCA), San Diego, June 2007

“ReCycle: Adaptive Pipelining for Tolerating Process Variation.” Invited talk at the Indian Institute of Technology (IIT), Guwahati, December 2007

PROJECTS

ReCycle: Adaptive Pipelining for Variation Tolerance

- Guide: Prof. Josep Torrellas, University of Illinois at Urbana-Champaign

Implemented Interprocedural Alias Analysis in the LLVM C/C++ compiler

- One of the two best projects in the course
- Instructor: Prof. Vikram Adve, University of Illinois at Urbana-Champaign

Phoenix: Fault tolerance framework for processor design bugs

- Guide: Prof. Josep Torrellas, University of Illinois at Urbana-Champaign

Register passing framework for thread level speculation (TLS) on SMT

- Worked with cycle-accurate simulator in C++ (SESC)
- Guide: Prof. Josep Torrellas, University of Illinois at Urbana-Champaign

Design and implementation of multihop wireless network testbed

- C++ programming
- Guide: Prof. Nitin Vaidya, University of Illinois at Urbana-Champaign

PasToC: A PASCAL to C converter

- Developed in C++
- Guide: Prof. S. K. Agarwal, IIT Kanpur

RELATED COURSEWORK

Advanced Topics in Compiler Construction (CS526) Parallel Computer Architecture (CS533)

Computer Microarchitecture (ECE512)

Distributed Systems (CS428)

Communication Network Analysis (ECE467)

Pattern Recognition and Machine Learning (CS446)

Machine Learning and Natural Language (CS598DNR)

SERVICE

Paper reviewer for ISCA and HPCA

Member of IEEE

STATUS

Citizen of India, holding an F-1 visa.

REFERENCES

- **Prof. Josep Torrellas**, UIUC
torrellas@uiuc.edu
- **Prof. Marc Snir**, UIUC
snir@uiuc.edu

- **Prof. Sarita V. Adve**, UIUC
sadve@uiuc.edu
- **Prof. Sanjay J. Patel**, UIUC
sjp@uiuc.edu
- **Dr. Christopher J. Hughes**, Intel Research
christopher.j.hughes@intel.com
- **Dr. Pradip Bose**, IBM Research
pbose@us.ibm.com