Morphable Multithreaded Memory Tiles (M3T)

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Architecture

M3T Architecture
- 64 Processing Cores
- 48 MB L1 cache
- 300 GB SDRAM
- AMD 80560 SP
- No explicit ordering
- Morphologic SIMD, VLIW, TaskScalar, and Stream

TaskScalar Morph
- User-level thread management
- All tasks are canceled by interrupt to user space

TaskScalar Morph Evaluation
- Applications: Matrix multiplication, 3D rendering, 80560 SP
- Bubble: Application with explicit task overlap that contains global activity
- Pathological: Application with all activity originating from the same core

Compiler Support

Novel compiler algorithms to build tasks
- Front End
- High Level Transformations
- Task Selection
- Inter-Task Optimizations
- Intra-Task Optimizations
- Code Generation

Software Productivity

Debugging Data Races [ISCA03]
- Task X
- Task Y
- [CPU]
- [IPC]
- [SMT]
- [Supercall]
- No explicit order between and

Reducing Parallel Programming Effort [ASPLOS92]
- Speculative Barrier
- Speculative Lock
- [TaskScalar Hardware]
- [No TaskScalar Hardware]
- Man-Hour Invested Programming

Overhead
- Redefinition Distance (instructions per CPU)
- [Detect]
- [Reduction]
- [Analyze]
- [Match]
- [Effective]
- [Speedup]