UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH

Fraunhofer
IZM

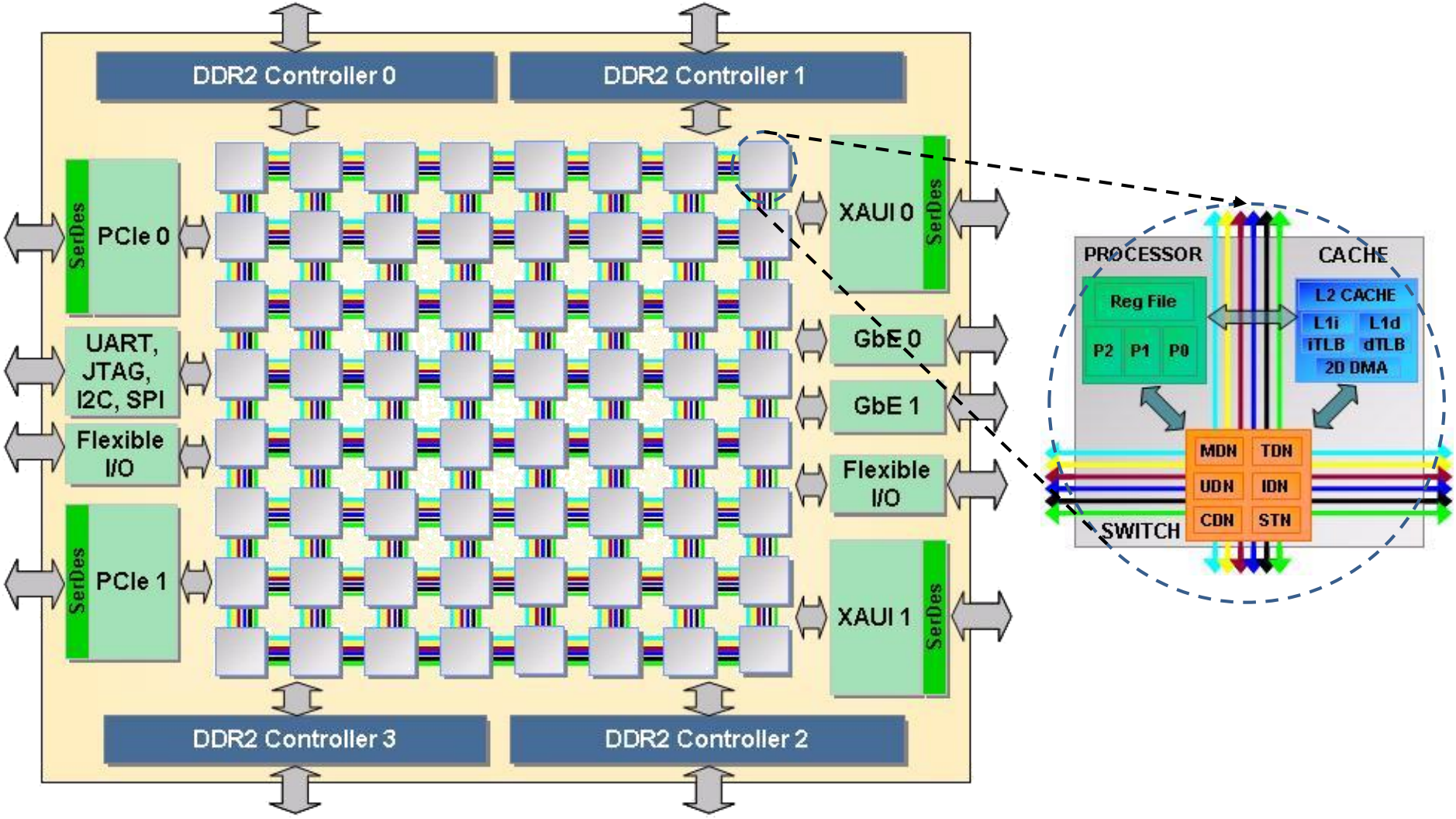
Millimeter-Wave Propagation within a Computer Chip Package

Sergi Abadal (abadal@ac.upc.edu)

Xavier Timoneda, Albert Cabellos-Aparicio, Dionysios Manessis, Jin Zhou, Antonio Franques, Josep Torrellas, Eduard Alarcón

IEEE International Symposium on Circuits & Systems (IEEE ISCAS)
Firenze – May 30th, 2018

Background: Multiprocessors

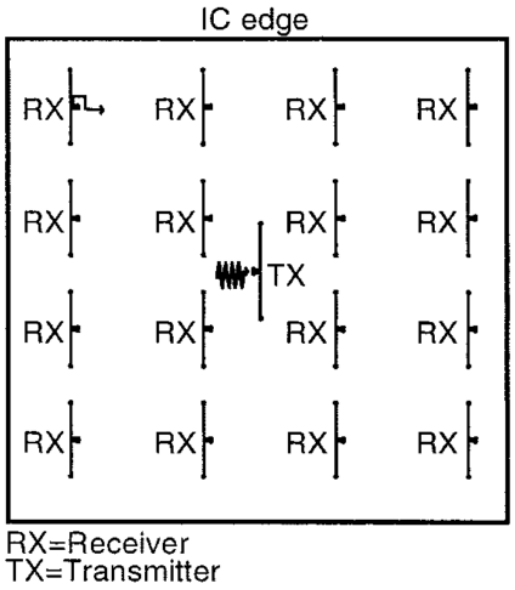


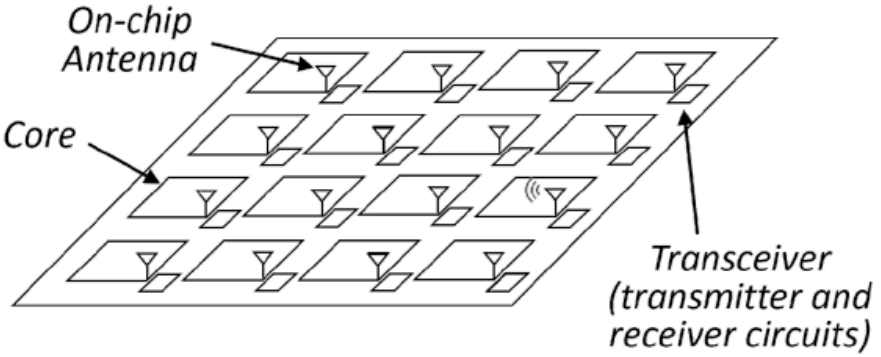
Background: Network-on-Chip

- Networks-on-Chip (NoCs) replaced buses to scale processors to 10s of cores
- However, they have their own problems when scaled further
  - Overprovisioning (rigidity)
  - Latency and energy for certain flows
- Need for alternatives or complements in the upcoming the kilo-core era (perhaps with emerging technologies...)

Background: Wireless NoC

- Advent of on-chip antennas opened new perspectives
- We can leverage them to implement wireless intra-chip communication in manycores
  - Naturally broadcast
  - Low latency
  - Flexibility

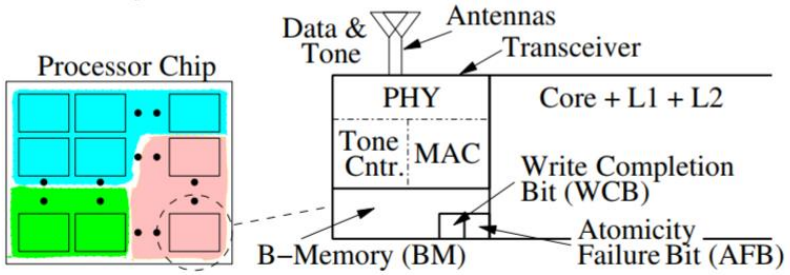


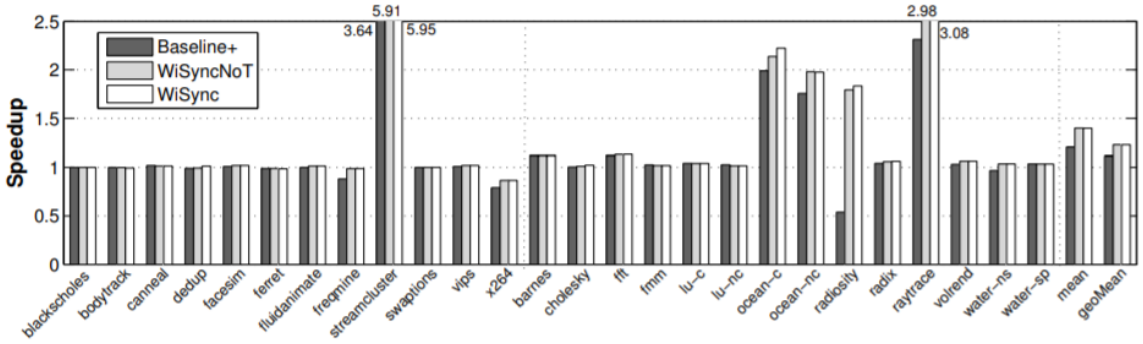


S. Deb, A. Ganguly, P. P. Pande, B. Belzer, and D. Heo, "Wireless NoC as Interconnection Backbone for Multicore Chips: Promises and Challenges," *IEEE J. Emerg. Sel. Top. Circuits Syst.*, vol. 2, no. 2, pp. 228–239, 2012.

Multiprocessor Architecture

- With small changes in the architecture of a manycore, we can leverage WNoC to achieve:
  - 43% average computation speedup in widely known benchmarks
  - Up to 5X in some cases
  - Potential to be even better
  - Reasonable overhead

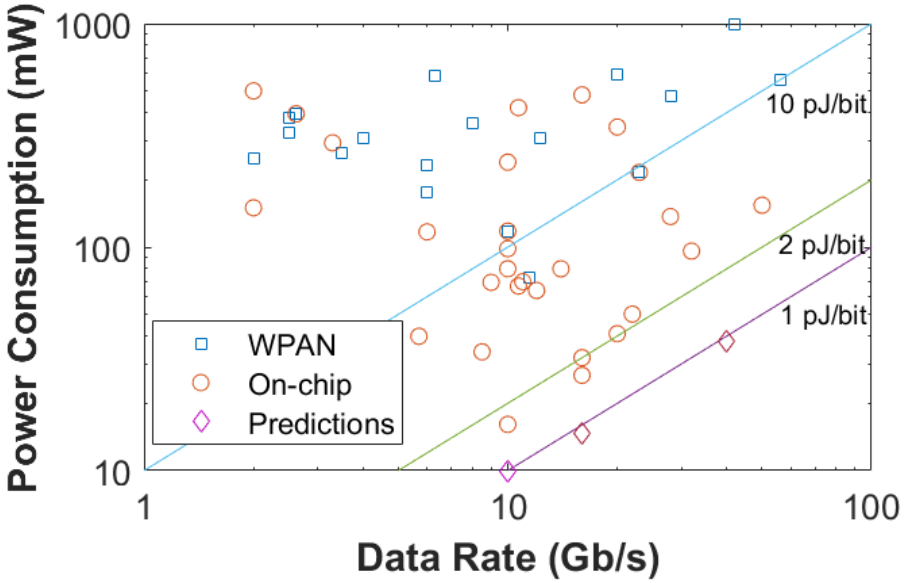


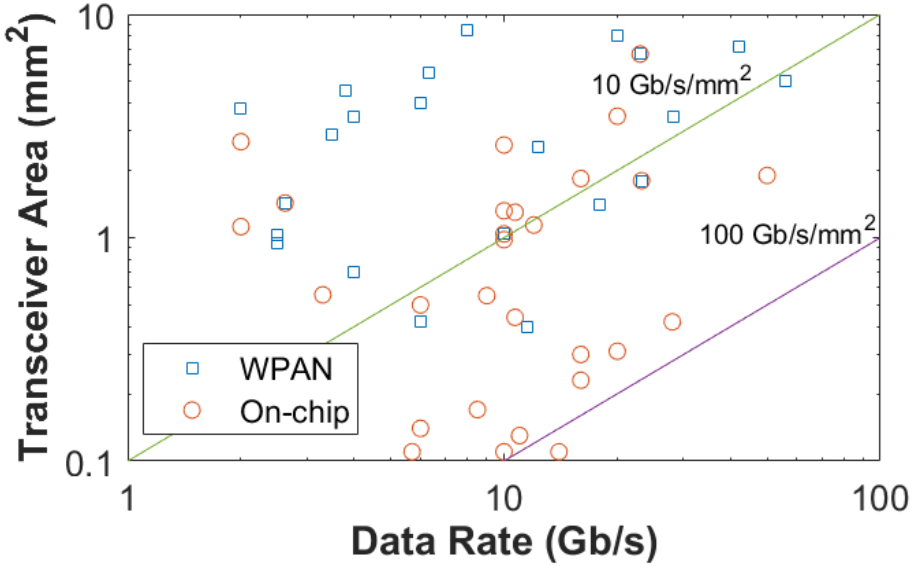


S. Abadal, E. Alarcón, A. Cabellos-Aparicio, and J. Torrellas, "WiSync: An Architecture for Fast Synchronization through On-Chip Wireless Communication," in Proceedings of ASPLOS, April 2016.

Integrated RF Transceivers

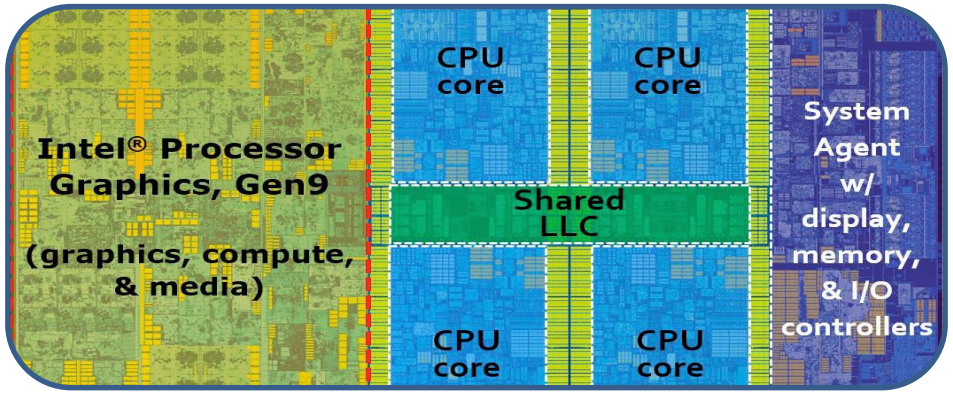
- For the WNoC idea to make sense, we need
  - 10+ Gbps
  - ~1 pJ/bit
  - ~100 Gb/s/mm^2
- Transceiver design is getting up to speed





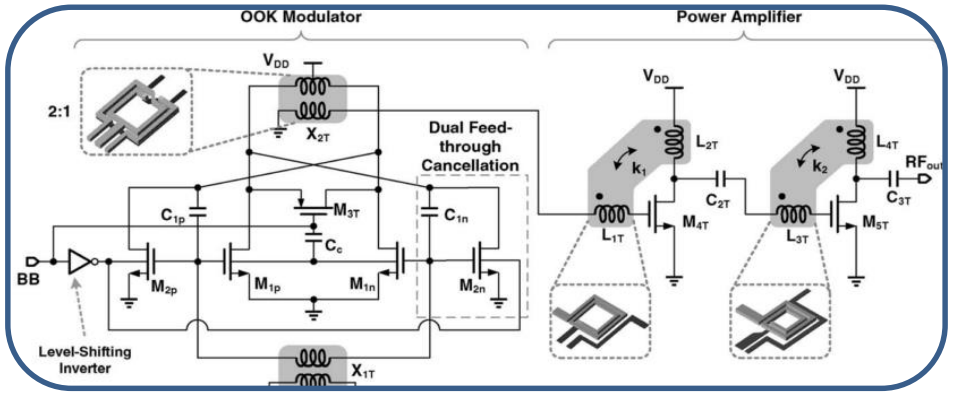
S. Abadal, M. Iannazzo, M. Nemirovsky, A. Cabellos-Aparicio, H. Lee, E. Alarcón,"On the Area and Energy Scalability of Wireless Network-on-Chip: A Model-based Benchmarked Design Space Exploration," IEEE/ACM Transactions on Networking, vol. 23, no. 5, pp. 1501-1513, Oct. 2015.

Motivation



Multiprocessor Architecture

Challenges



Integrated RF Transceivers

Motivation

- The intra-chip wireless channel is relatively unknown – transceiver testing:
  - Loopback, or
  - Freespace conditions
  - Generally without chip package
- We thus cannot ensure having 10+ Gbps and 1 pJ/bit as expected–required
- There is a need to understand the chip package effects on propagation

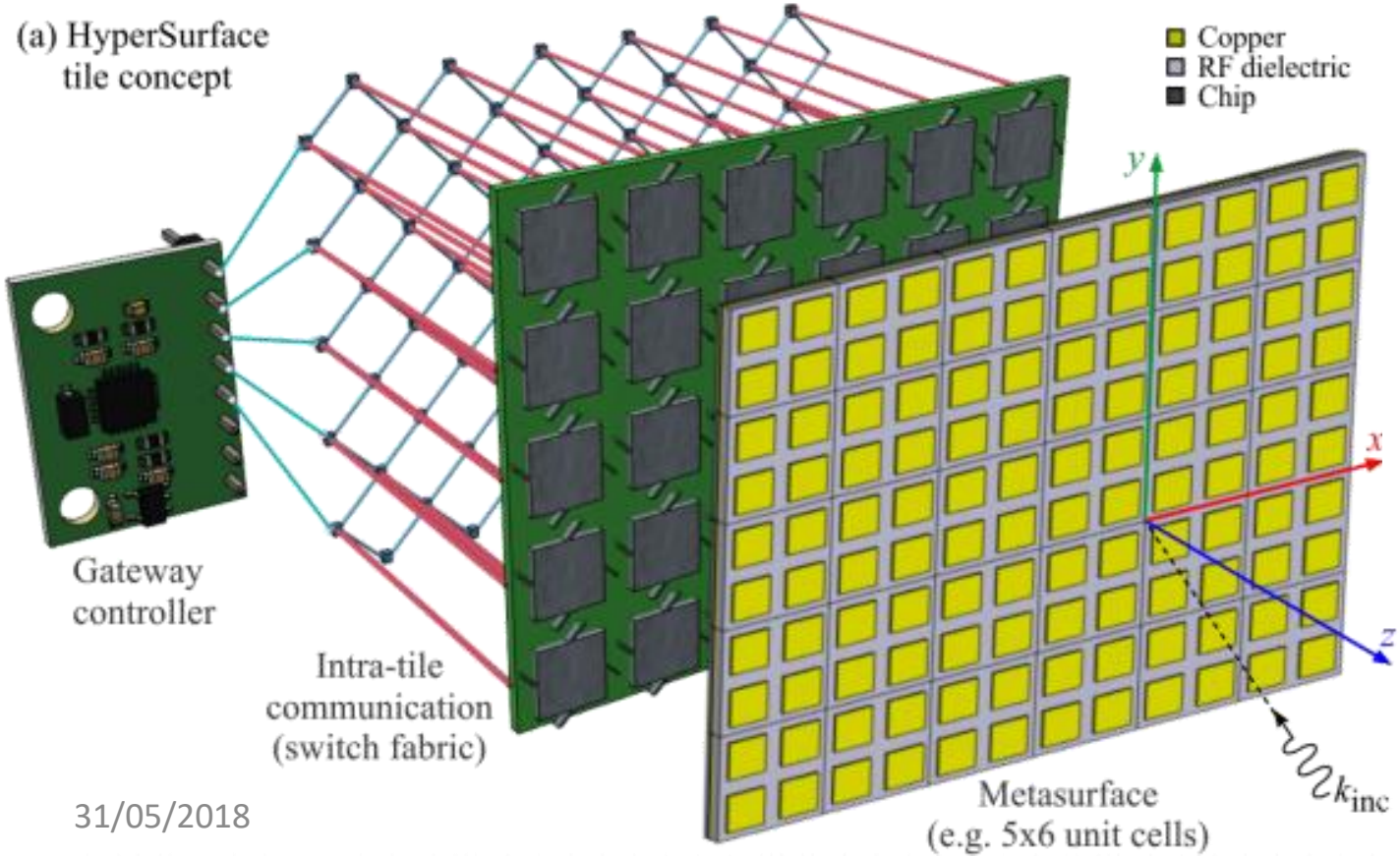
Contribution

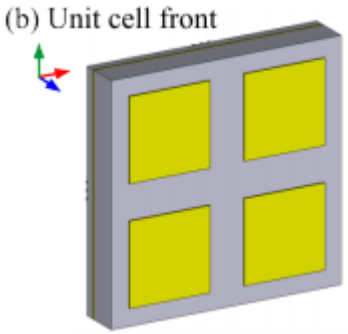
- We investigate wave propagation within a realistic chip package model
- Through full-wave simulations, we extract path loss figures (and trends)
- We demonstrate that tweaking several parameters of the package we can minimize losses

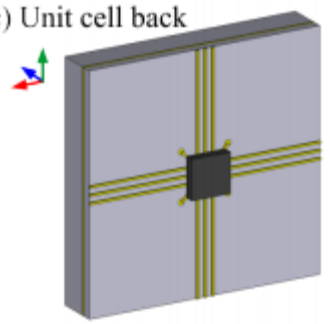
Why in this session?

METASURFACE HYPERVISOR

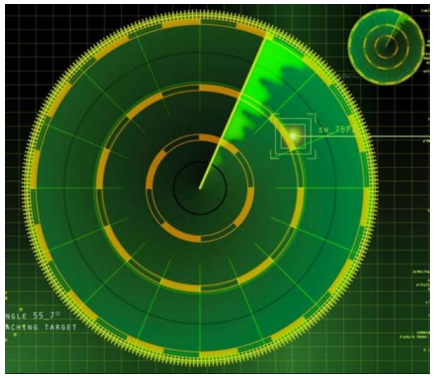
A Hardware Platform for Software-Driven Functional Metasurfaces

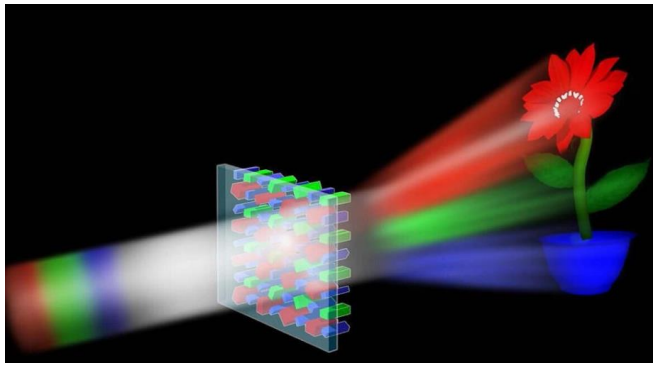


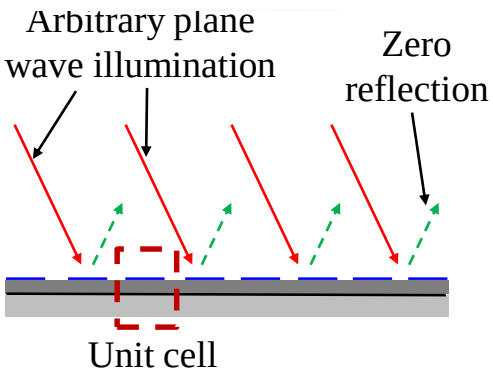


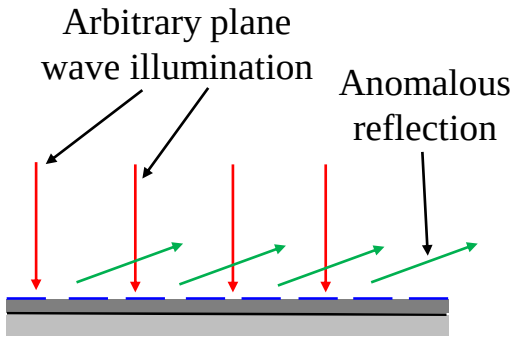


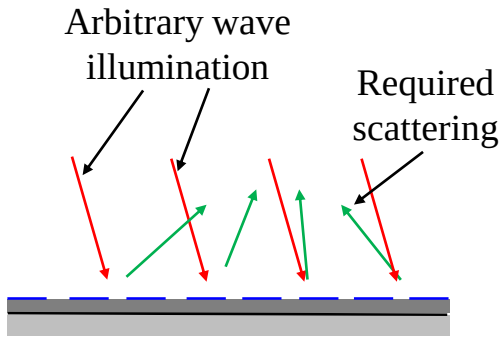
Why in this session?

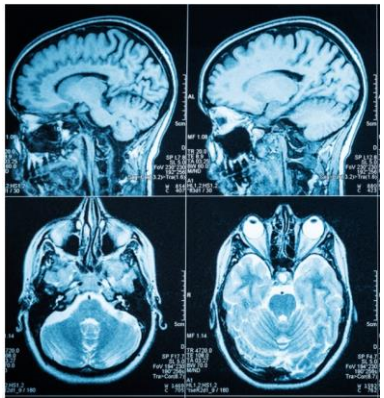


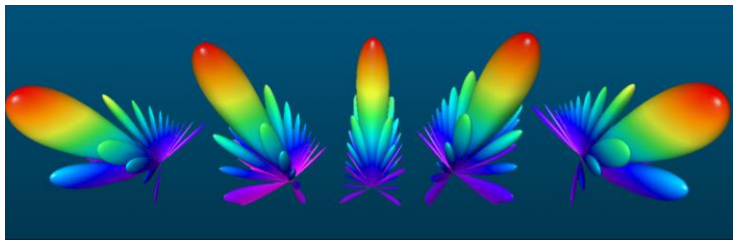


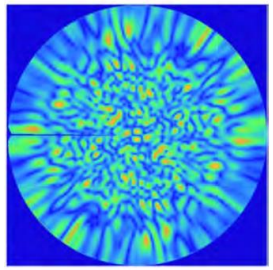


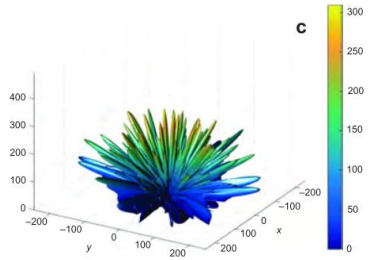








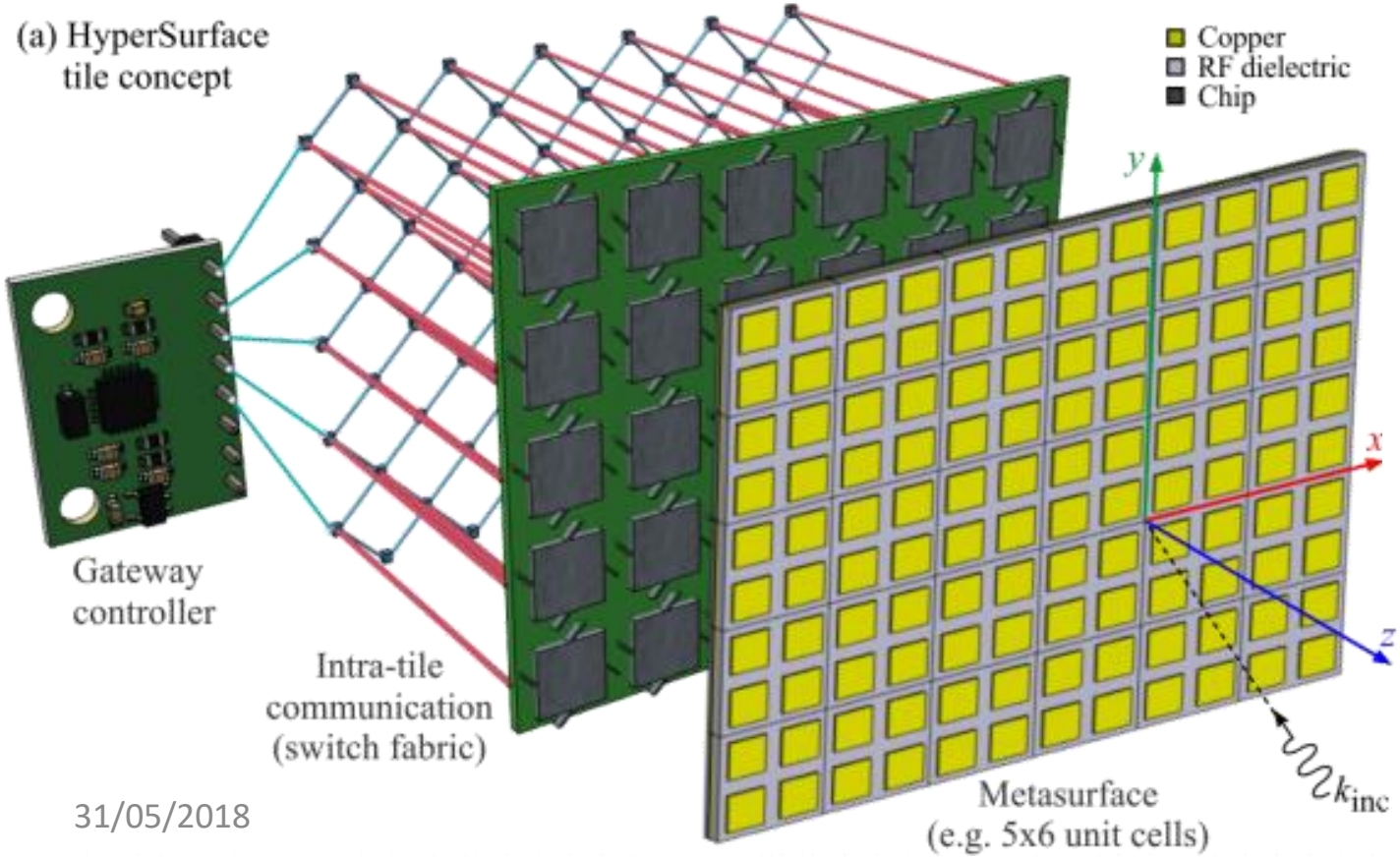


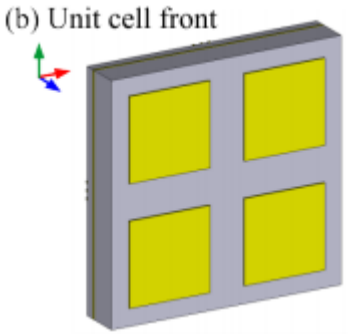


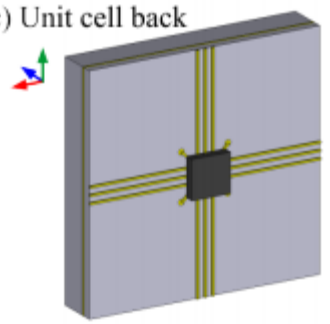
Why in this session?

METASURFACE HYPERVISOR

A Hardware Platform for Software-Driven Functional Metasurfaces



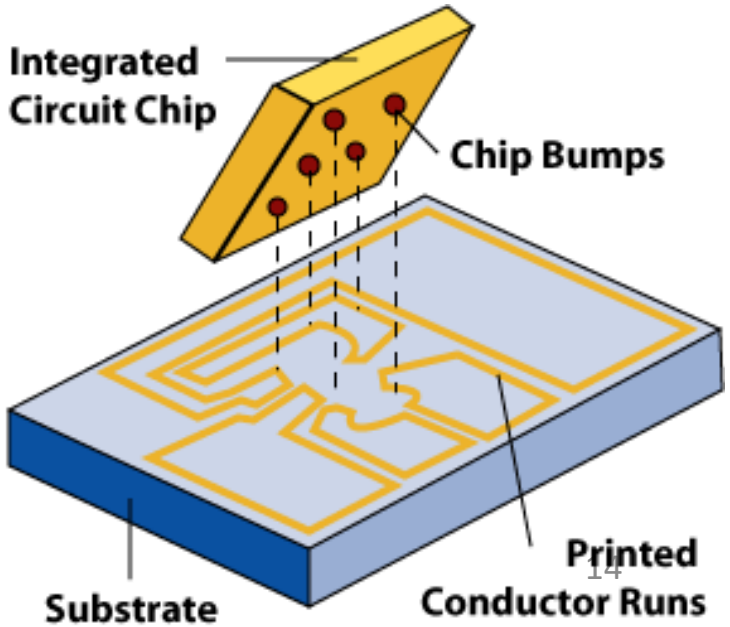




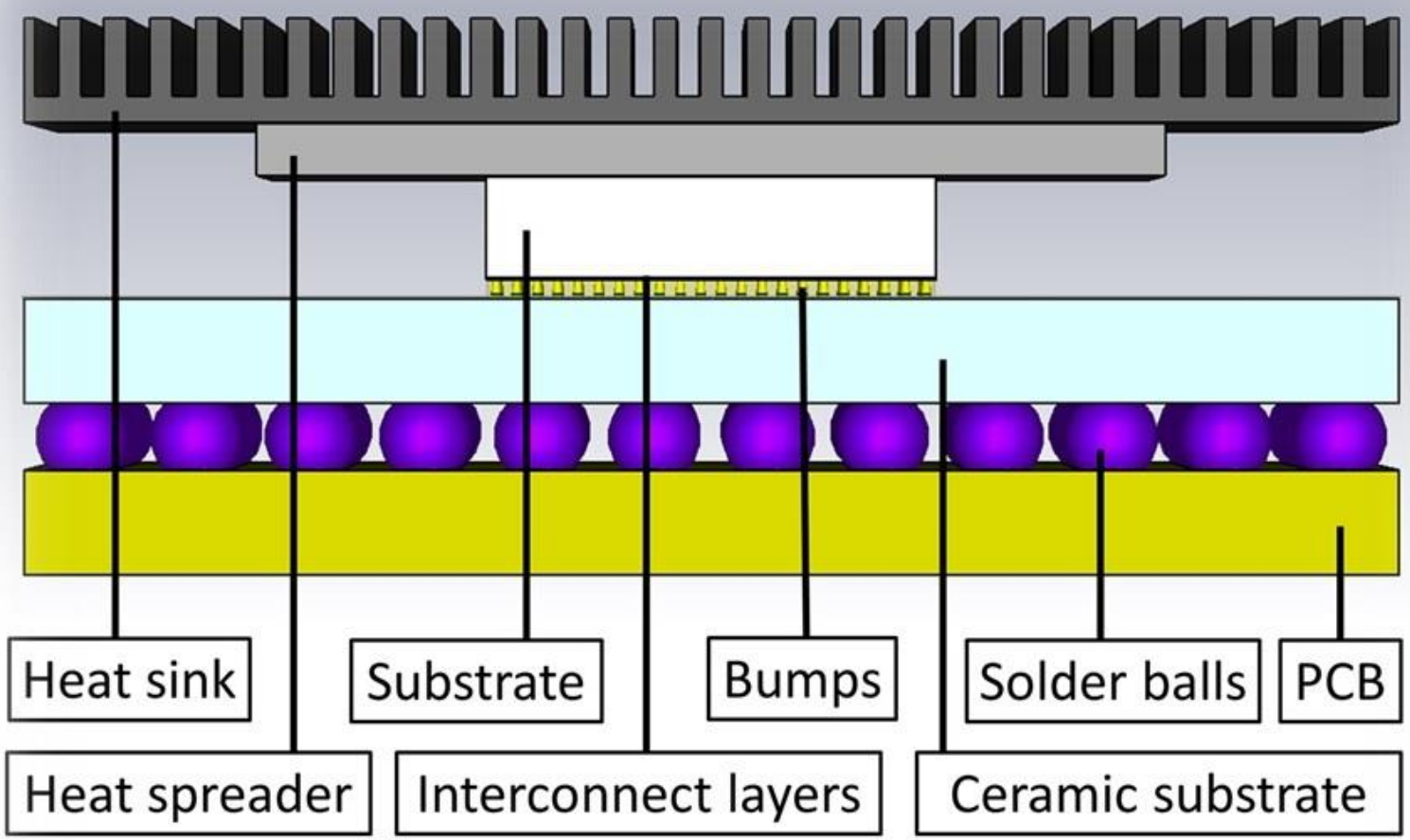
System Model

System Model

- We assume a flip-chip package, preferred over wire bonding because
  - Lower I/O signal inductance
  - Lower power-ground inductance
  - Higher power density

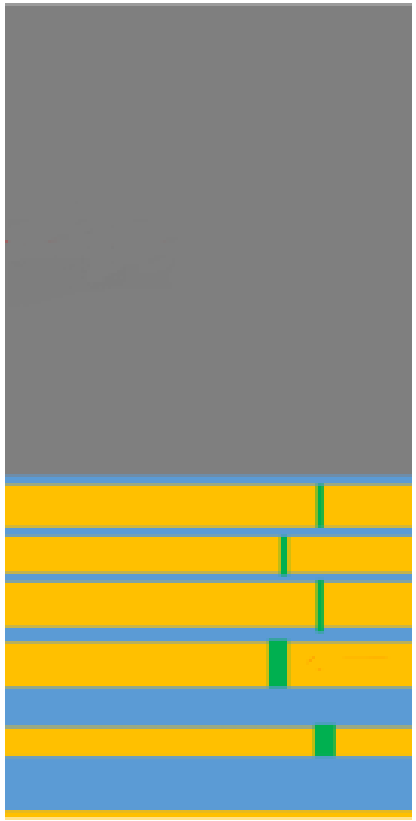


Anatomy of a flip-chip package



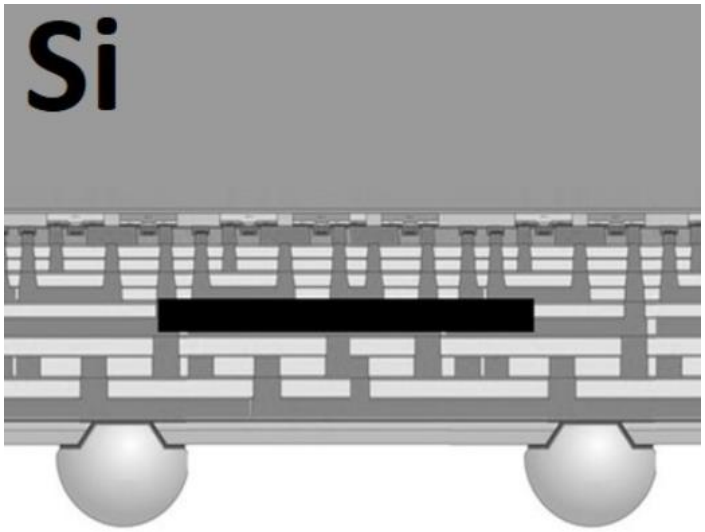
Antenna placement

- Three options
  - Planar, away from the silicon
  - Planar, close to the silicon
  - Vertical, through silicon



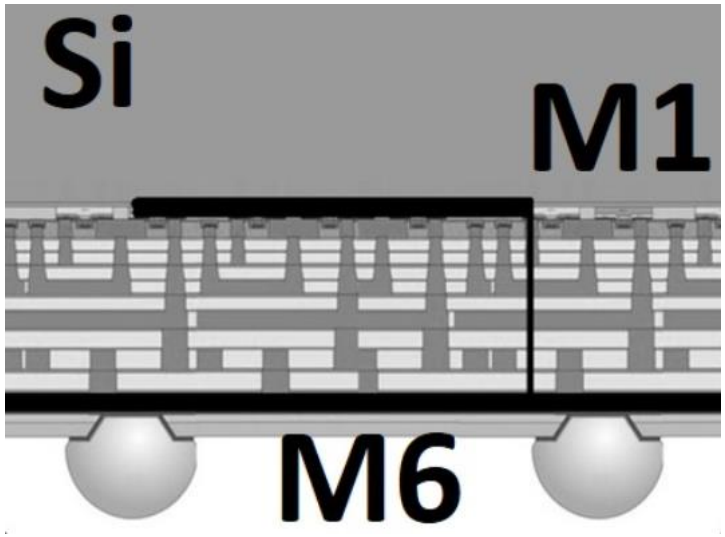
Types of antennas (I)

- Square aperture antenna
  - Electrically small, quasi-omnidirectional source, adequate for channel sounding
  - Placed within the insulator



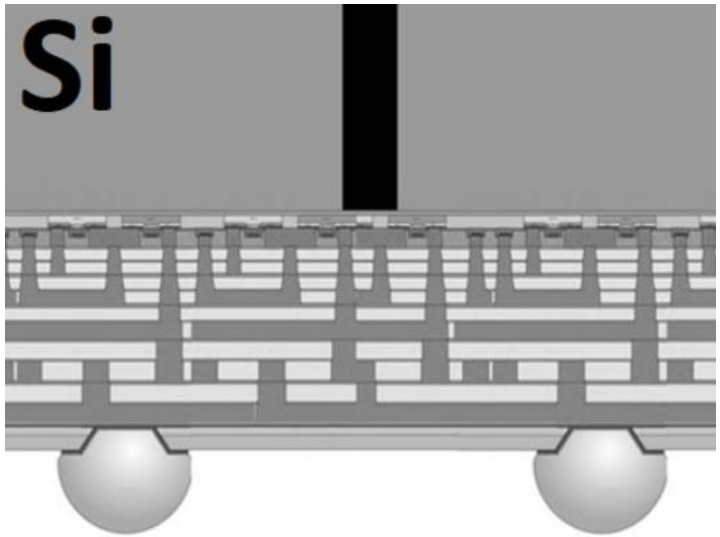
Types of antennas (II)

- Patch antenna
  - More realistic planar antenna
  - M1 for patch and M6 for ground



Types of antennas (III)

- Vertical monopole
  - Doable with through-silicon vias
  - Tuning is possible as length is adjustable with electropalating techniques



Methodology

Evaluation Methodology

- The whole package is introduced in a full-wave solver (CST)
  - Lateral dimensions: approx 500 mm^2 chip, approx 1000 mm^2 package
  - Metal layers are modeled as a solid metallic chunk (lateral and vertical separations are much smaller than wavelength)
- The antennas are also modeled, tuned to 60 GHz ($|S_{11}| < 10$ dB)

Main Parameters

TABLE I
CHARACTERISTICS OF THE LAYERS IN A COMPUTING PACKAGE

	Thickness	**Material**	ε_r	$\tan(\delta)$
Heat sink	0.5 mm	Aluminum	-	-
Heat spreader	0.25 mm	Thermal cond.	8.6	$3 \cdot 10^{-4}$
Silicon die	0.489 mm	Bulk Silicon	11.9	0.2517
Interconnections	13 µm	Cu and $\mathbf{SiO_2}$	3.9	0.03
Bumps	87.5 µm	Cu and Sn	-	-
Ceramic carrier	0.5 mm	Alumina	9.4	$4 \cdot 10^{-4}$
Solder balls	0.32 mm	Lead	-	-
PCB	0.5 mm	Epoxy resin	4	-

Frequency domain metrics

- Homogeneous distribution of 4 x 4 antennas within the chip
- We obtain field distribution and the S-params:

$$S_{ij}(f)\ \forall i,j \in [1,16], f \in [55,65]\ GHz$$

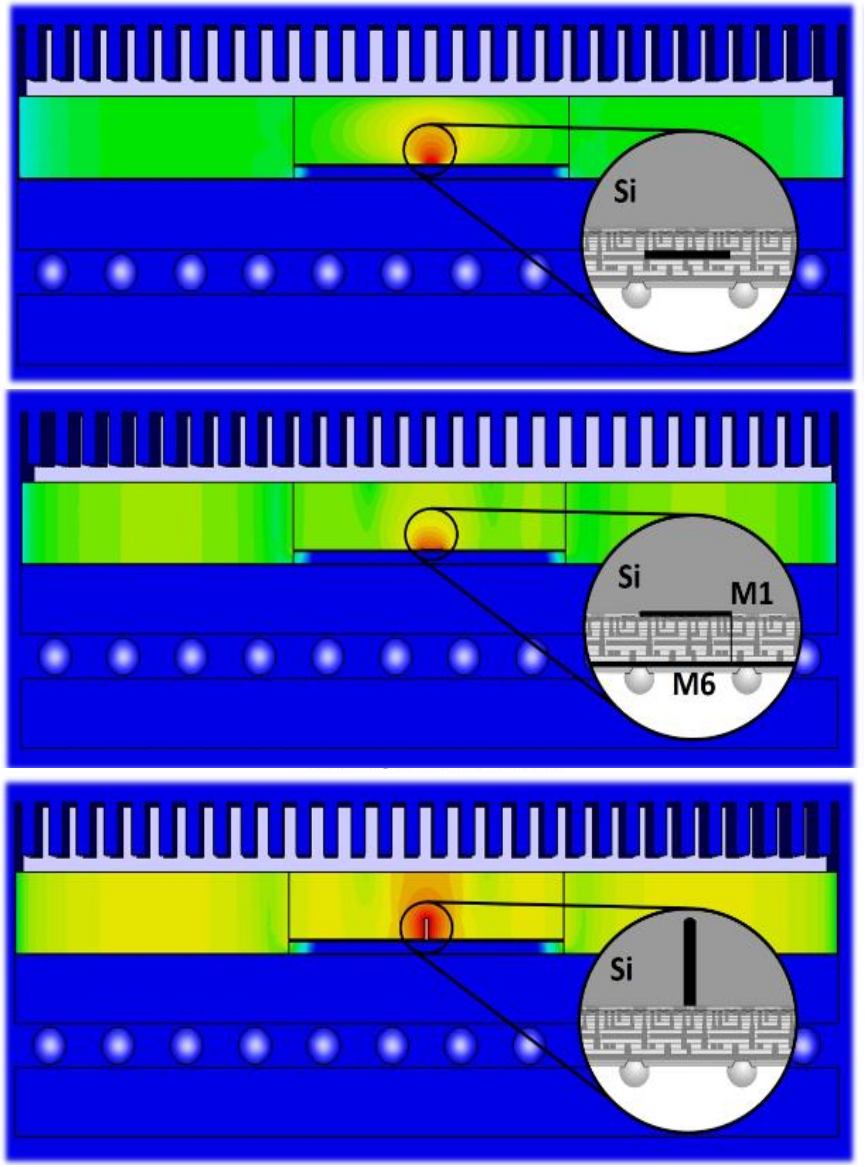
- If needed, we can obtain channel response decoupling the antenna effects

$$G_t G_r |H(f)|^2 = \frac{|S_{21}|}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$$

Results

Field distribution

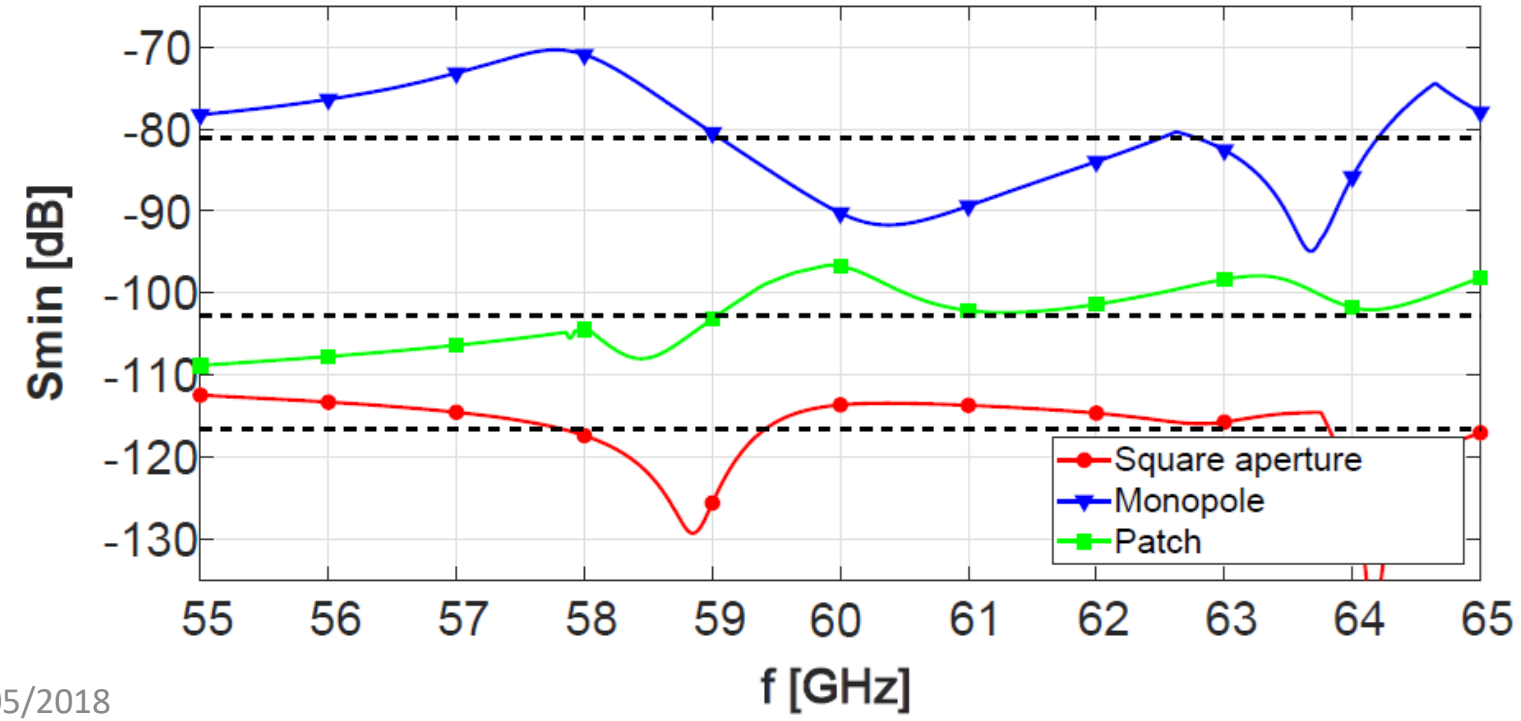
- **Ap:** grounded punctual excitation. Upwards, low eff
- **Pa:** a bit higher intensity, upwards and laterally
- **Mo:** higher lateral radiation, eff



Worst-case path loss

- The worst-case path loss is studied

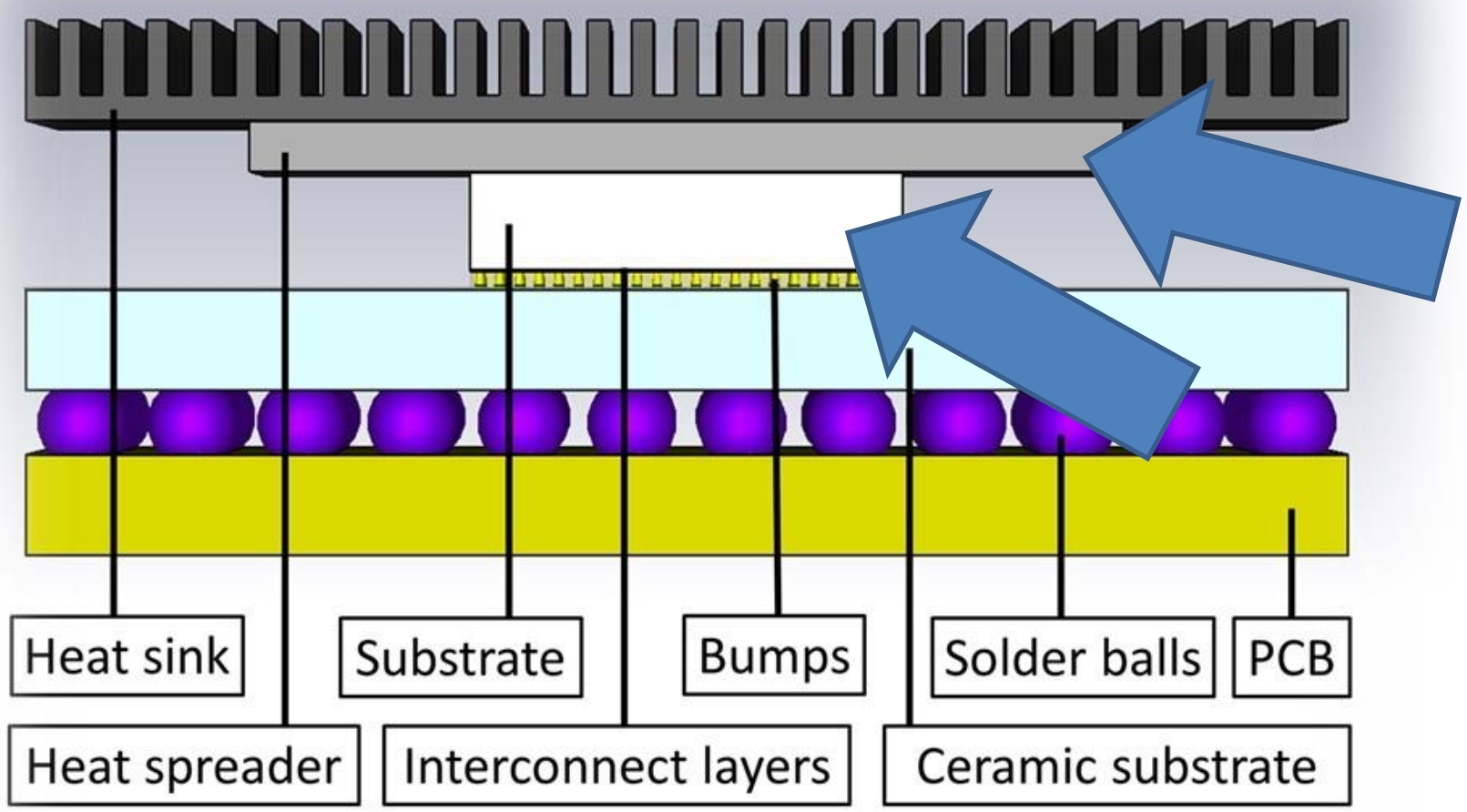
$$S_{min}(f) = \min_{i,j \neq i} S_{ij}(f)$$



Worst-case path loss

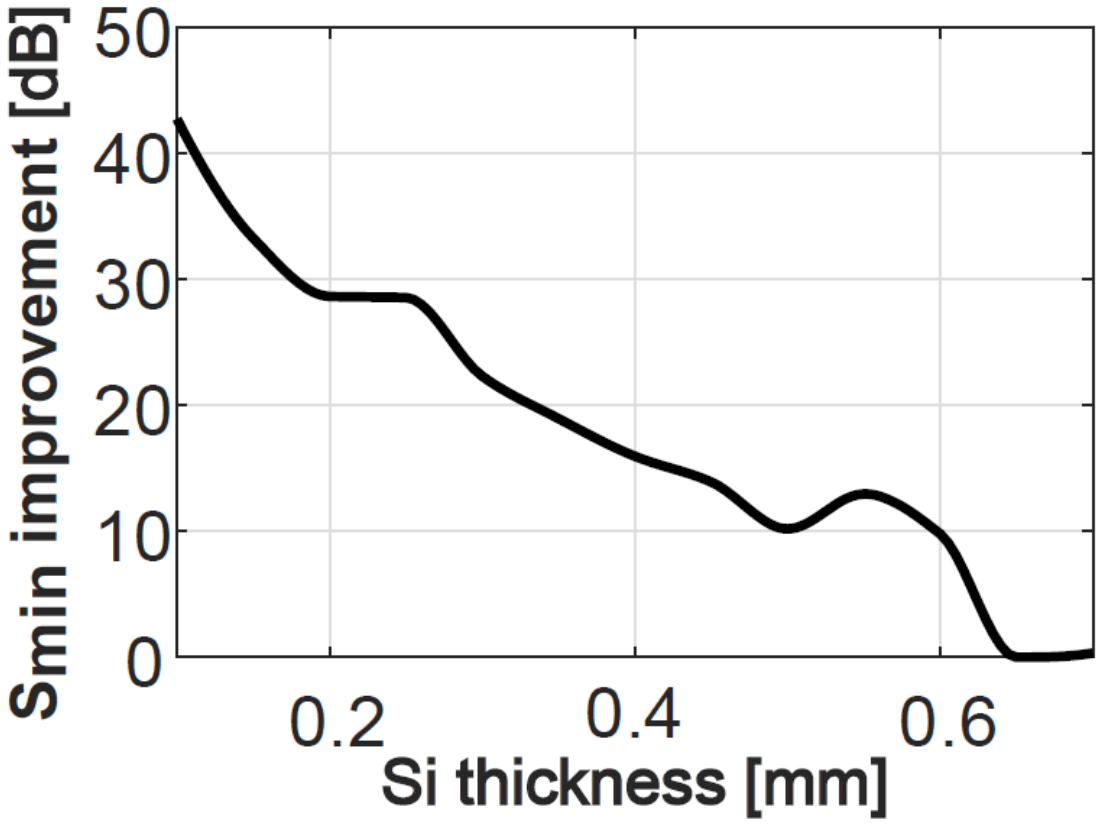
- Even in the most favorable case (vertical monopole) the attenuation is huge
- Normally one can improve the antenna, but this is hard / will have low impact here
- Instead, we can engineer the channel by modifing the package
  - Thinning the silicon
  - ~~Additional~~ Dielectric layer

Anatomy of a flip-chip package



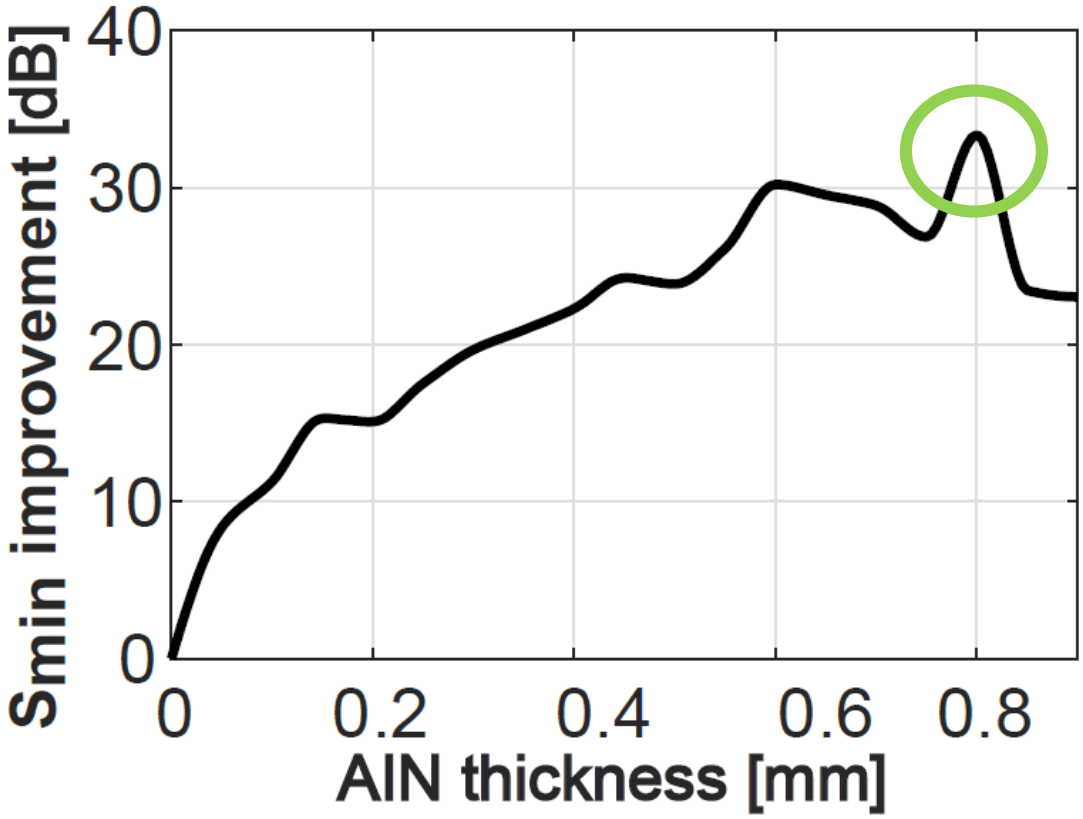
Thinning the silicon

- Improvement over regular silicon thickness (start at 0.7 mm)

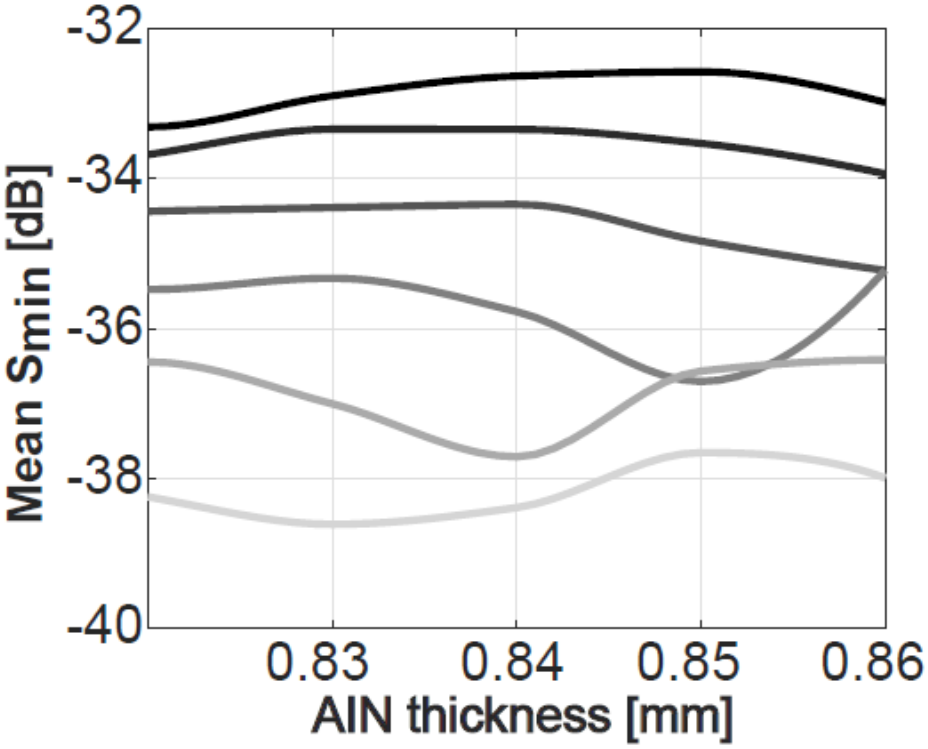


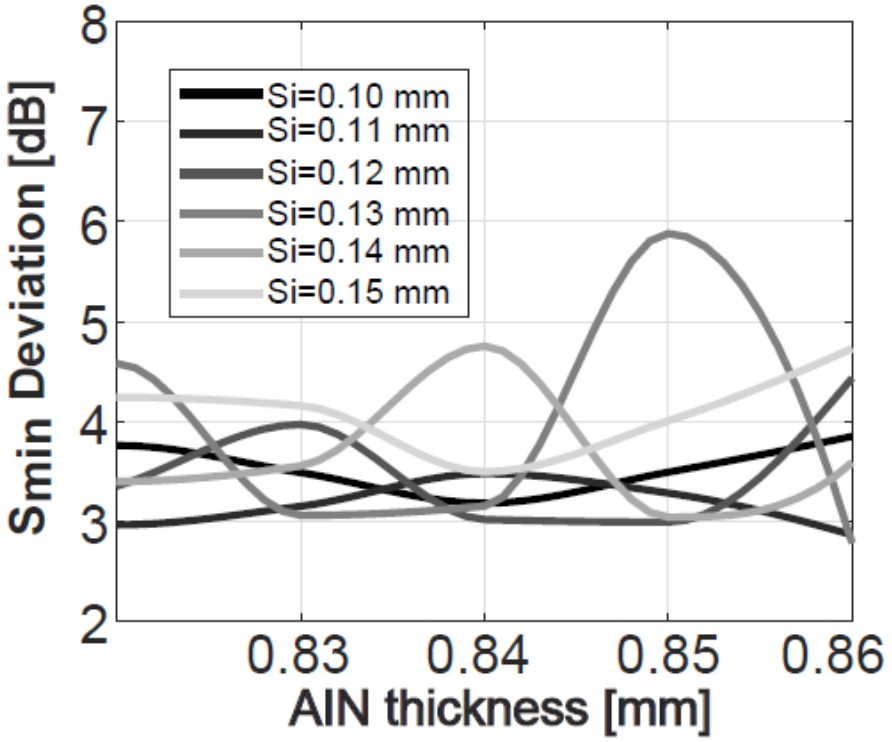
Dielectric layer

- Improvement over not having the dielectric (Aluminium Nitride, AlN)



Dielectric layer + thin silicon





Thin Si and thick AlN leads to maximum S_{min} with reasonable dispersion

Modeling the path loss

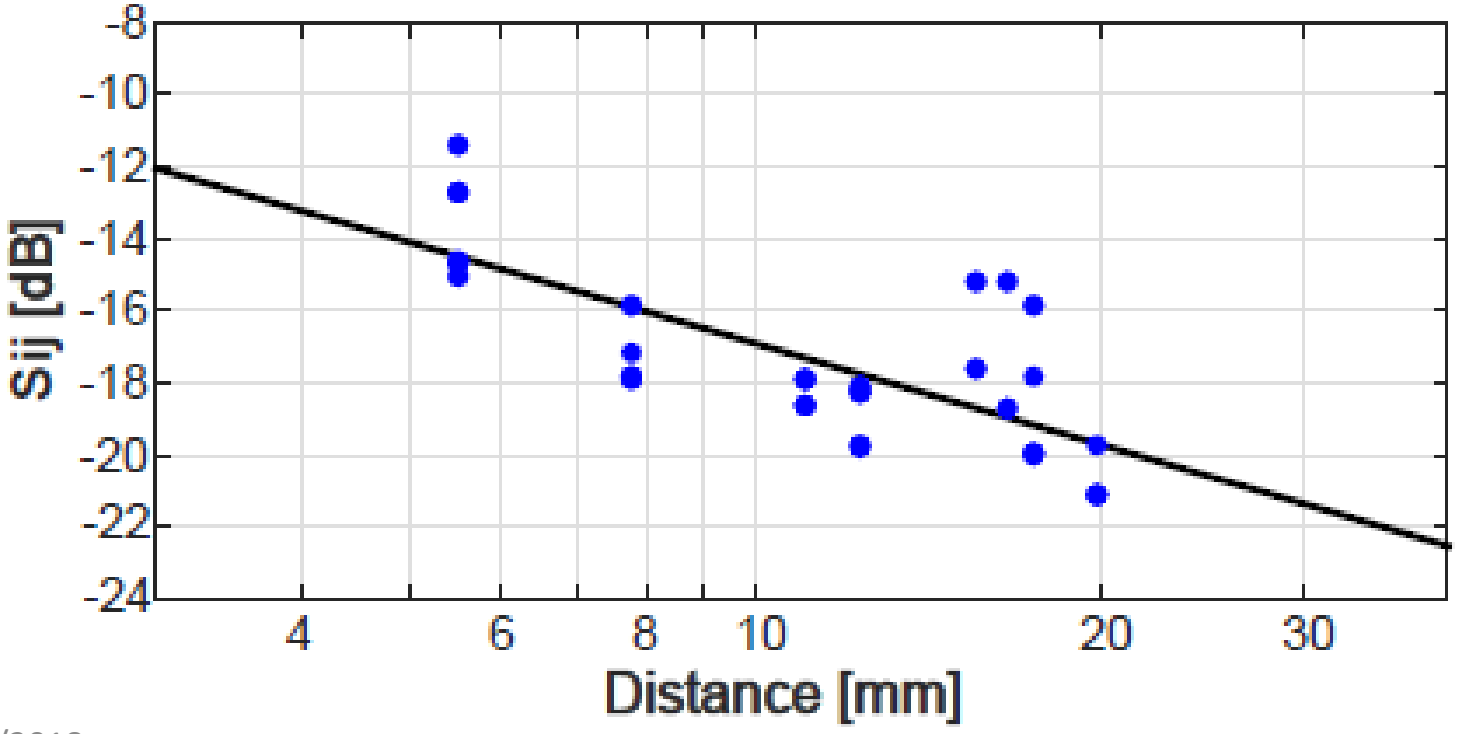
- The path loss exponent is obtained by doing a linear fitting of path loss (L) over distance (d) with the formula:

$$L_{db} = 10n \cdot \log_{10} d + C$$

  - n < 2 ➔ waveguide
  - n = 2 ➔ freespace, LoS
  - n > 2 ➔ lossy environment, NLoS

Modeling the path loss

- Fitting yields n = 0.932
  - Strong waveguiding effect (confinement)



Discussion

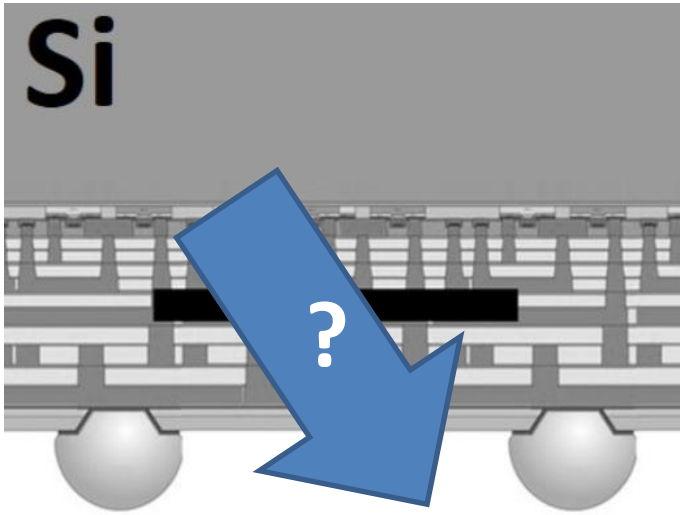
- The methodology is applicable to other scenarios and applications
  - System-in-Package
    - Mutichip modules
    - Heterogeneous CPU+GPU
  - Programmable metasurfaces

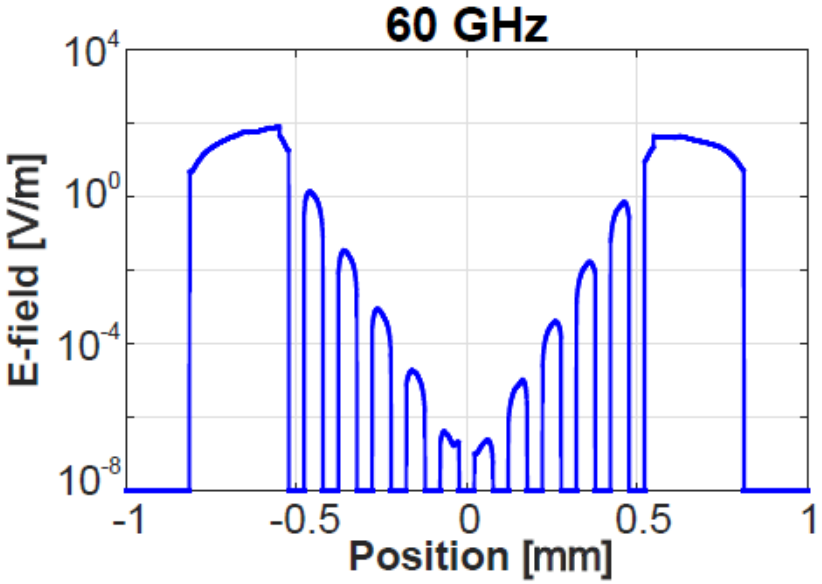
Discussion

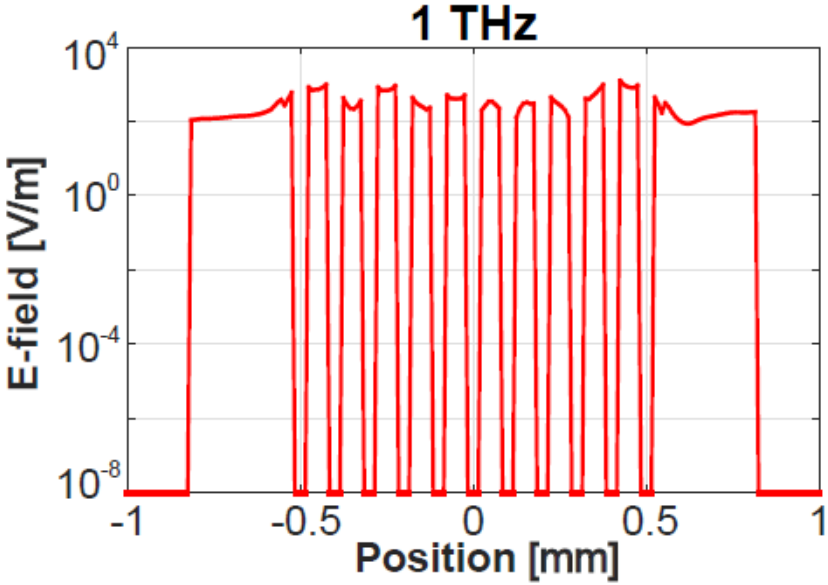
- Optimal design points will probably change with frequency for different reasons, including:
  - Behavior of materials at smaller wavelengths
  - Relative distances / spreading losses
  - Some obstacles may not be anymore as we reduce the wavelength

Scaling in frequency

- Fields will make their way through the bumps when wavelengths become commenurate to the bumps' pitch

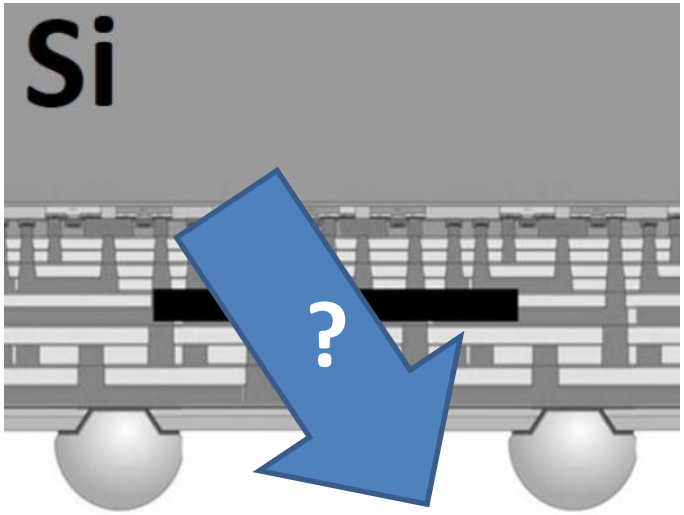


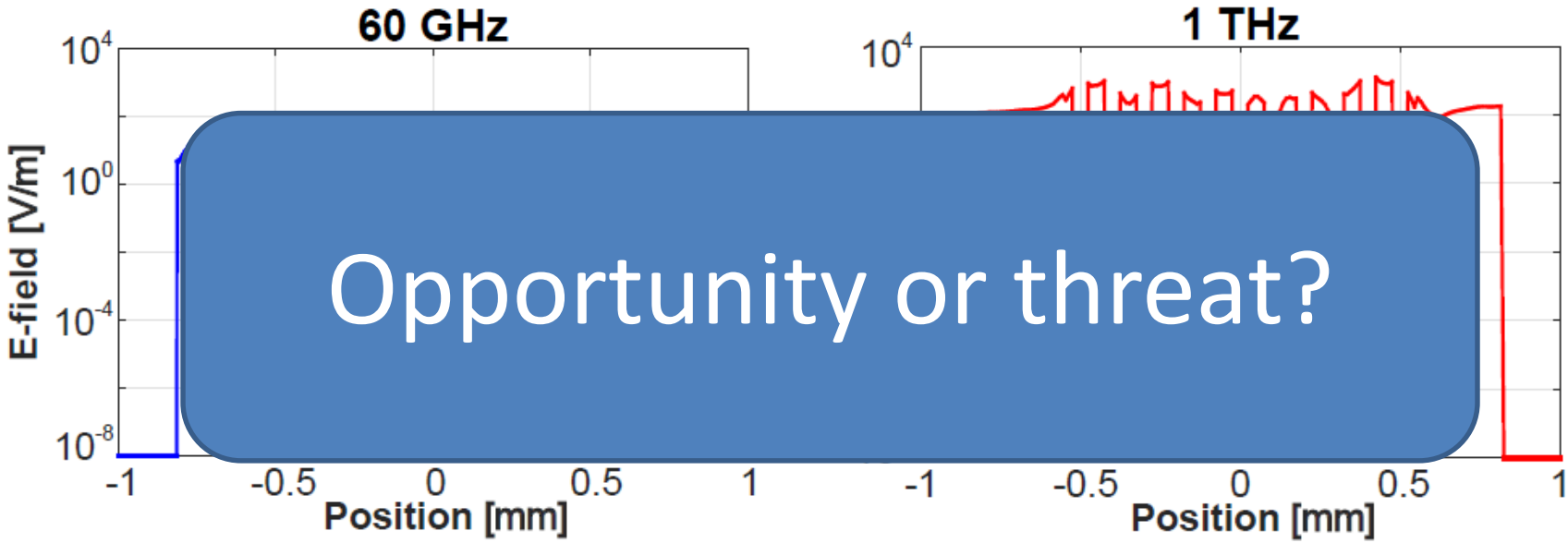




Scaling in frequency

- Fields will make their way through the bumps when wavelengths become commenurate to the bumps' pitch





Conclusions

- Vertical monopole shows promise for intra-chip wireless, but path loss is huge
- Through package optimization, 50 dB improvement in path loss is achieved
- Path loss exponent is around 0.9, which denotes high waveguiding effect
- Bump area propagation could be relevant at higher frequencies

Acknowledgments

FLAG-ERA

www.visorsurf.eu

Twitter

Facebook

This project has received funding from the European Union's Horizon 2020 research and innovation programme-Future Emerging Topics (FETOPEN) under grant agreement No 736876

UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH

Fraunhofer
IZM

Millimeter-Wave Propagation within a Computer Chip Package

Sergi Abadal (abadal@ac.upc.edu)

Xavier Timoneda, Albert Cabellos-Aparicio, Dionysios Manessis, Jin Zhou, Antonio Franques, Josep Torrellas, Eduard Alarcón

IEEE International Symposium on Circuits & Systems (IEEE ISCAS)
Firenze – May 30th, 2018