



# Runnemedede: an Architecture for Ubiquitous High-Performance Computing

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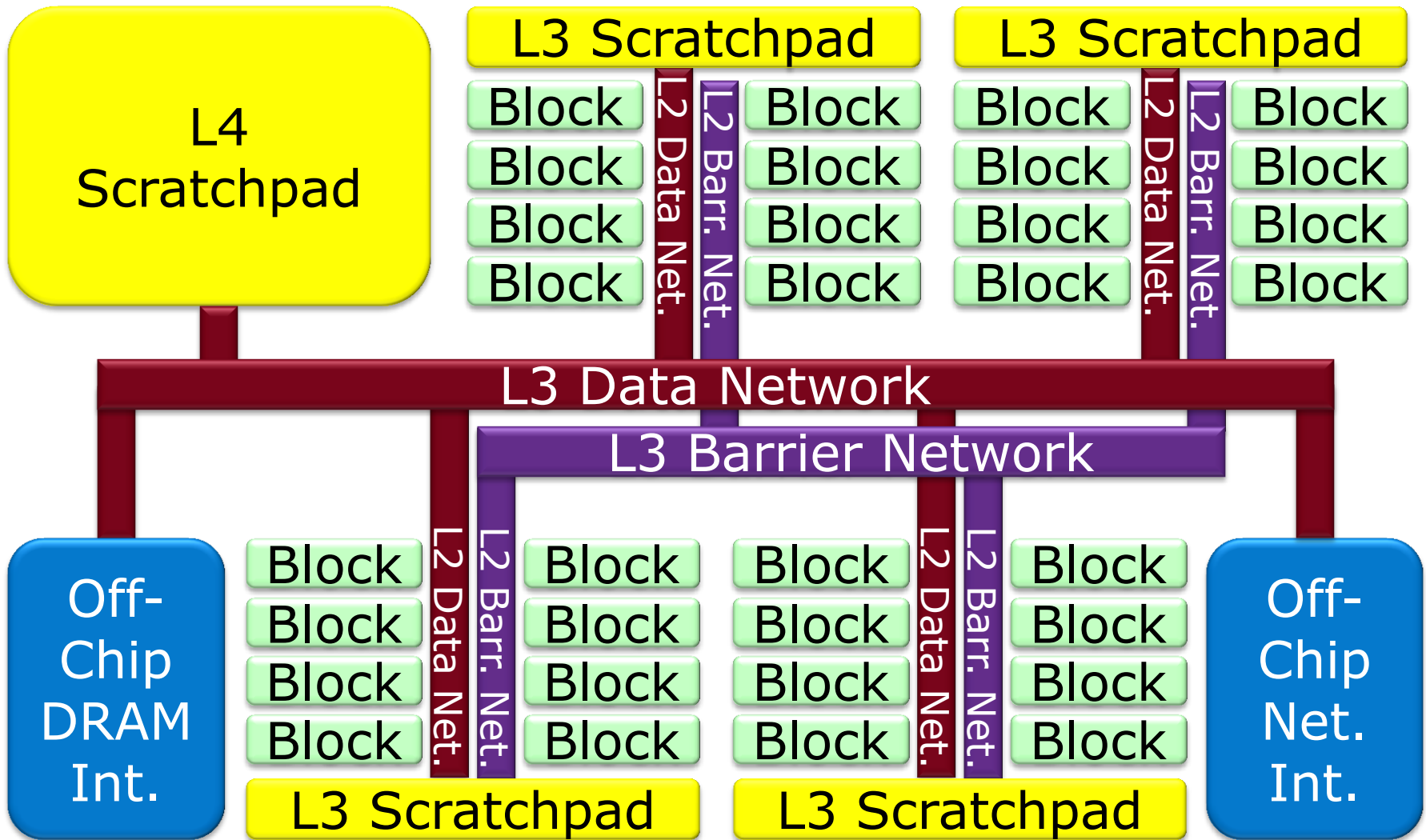
# DARPA UHPC Program

Runnemedde: Intel's UHPC research architecture

50 GOPS/Watt

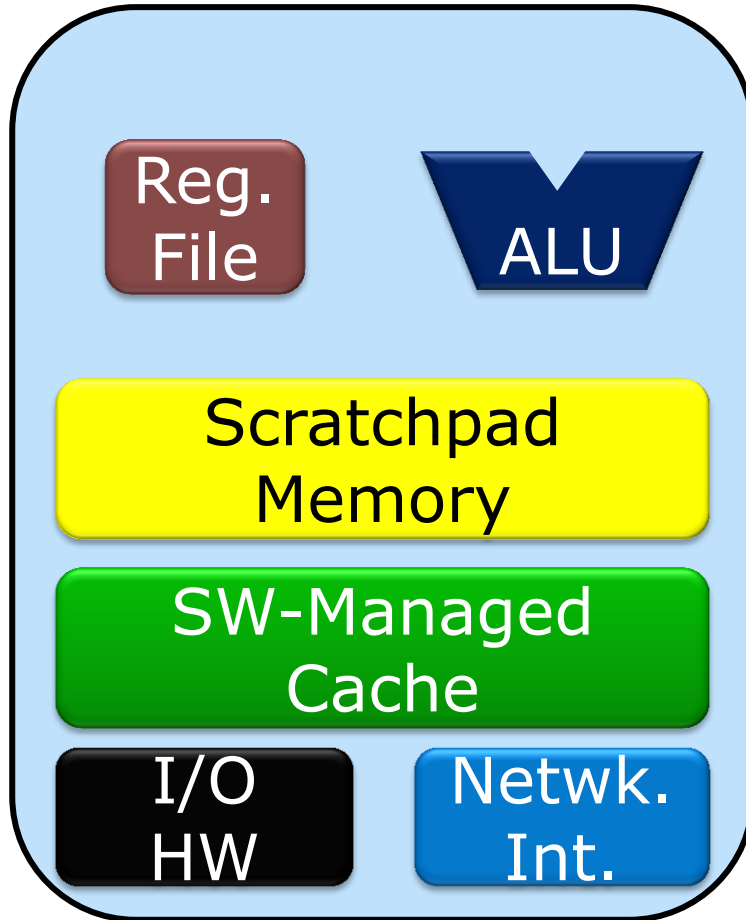
Ubiquitous

# A Runnemedede Chip

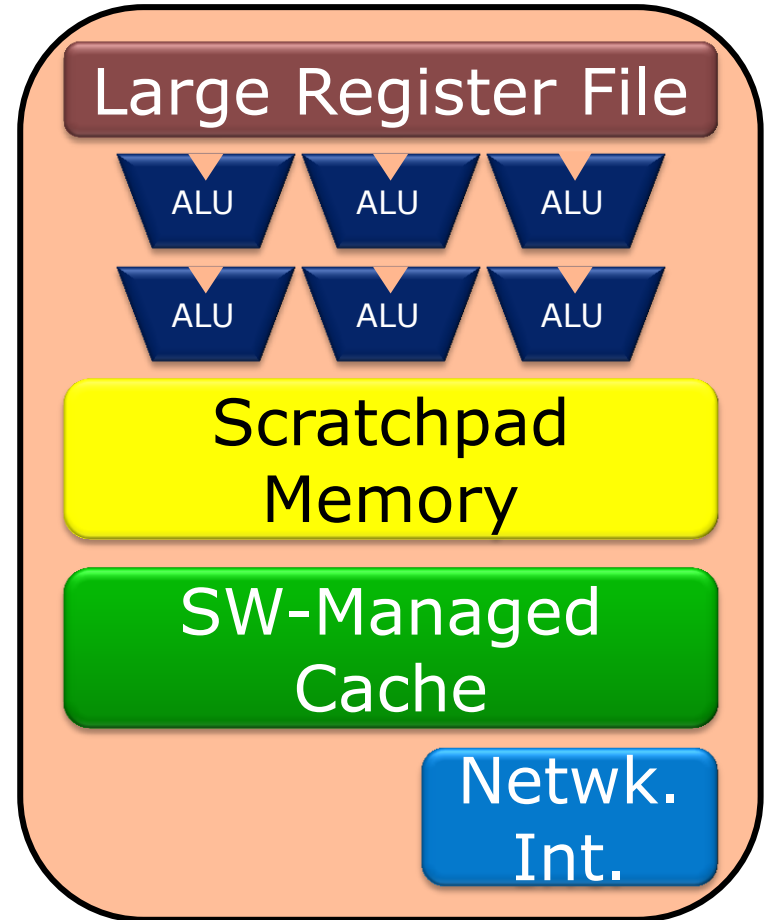


# Heterogeneous Cores

Control Engine (CE)



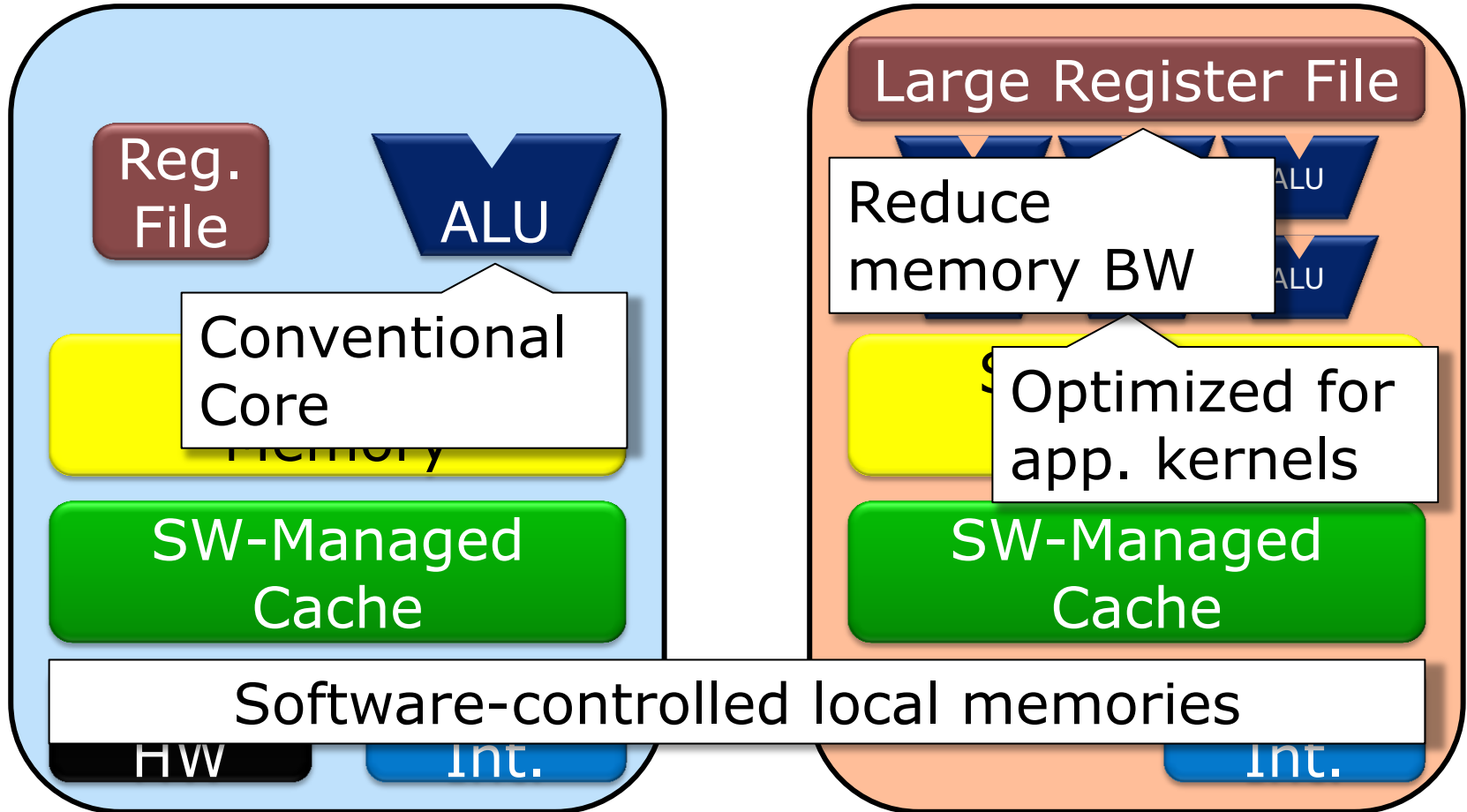
eXecution Engine (XE)



# Heterogeneous Cores

Control Engine (CE)

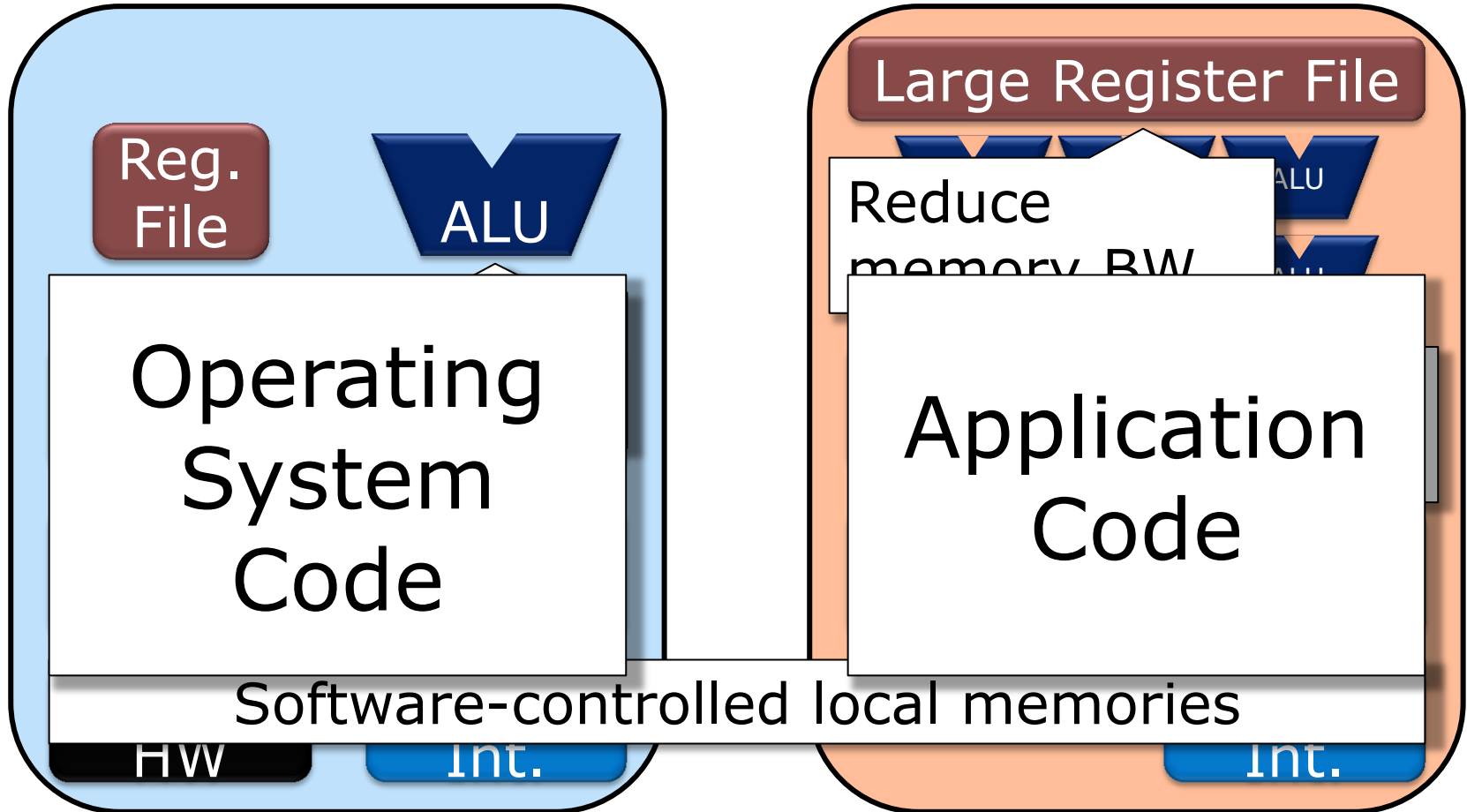
eXecution Engine (XE)



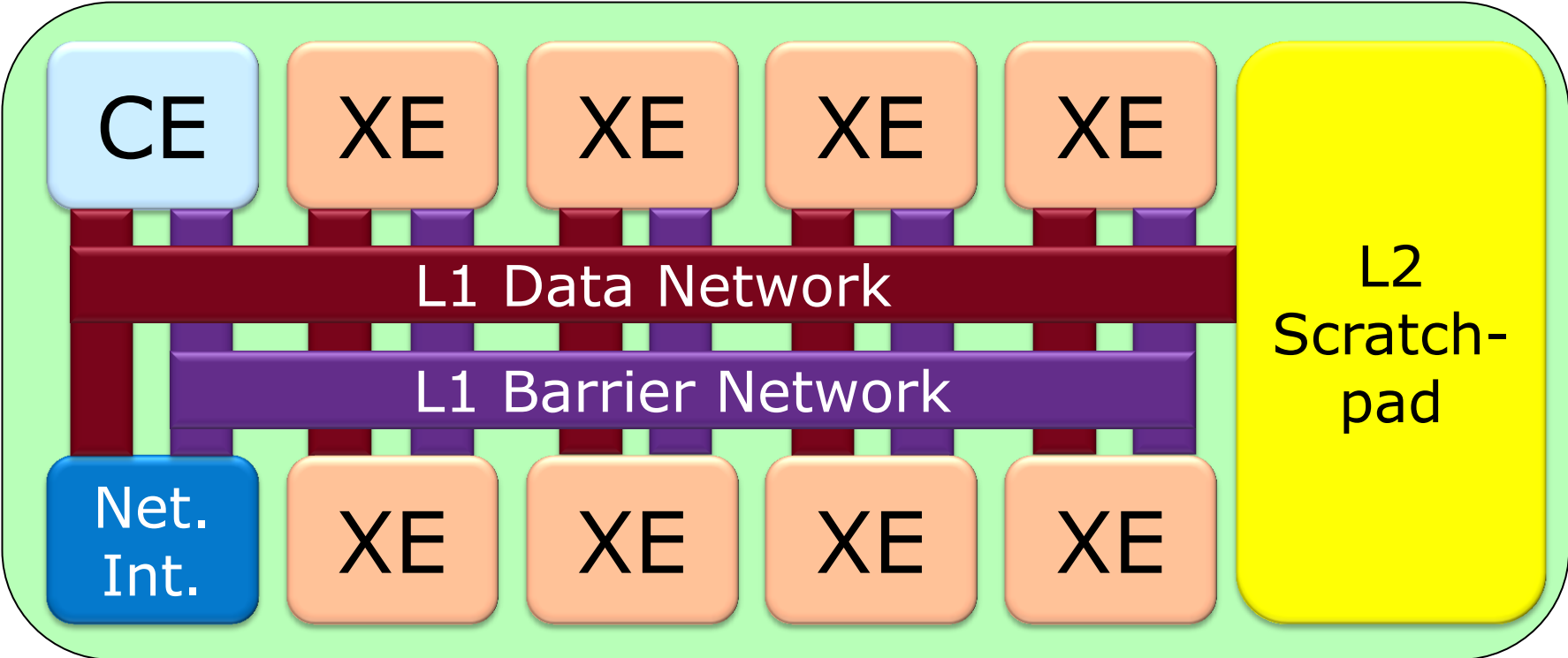
# Heterogeneous Cores

Control Engine (CE)

eXecution Engine (XE)

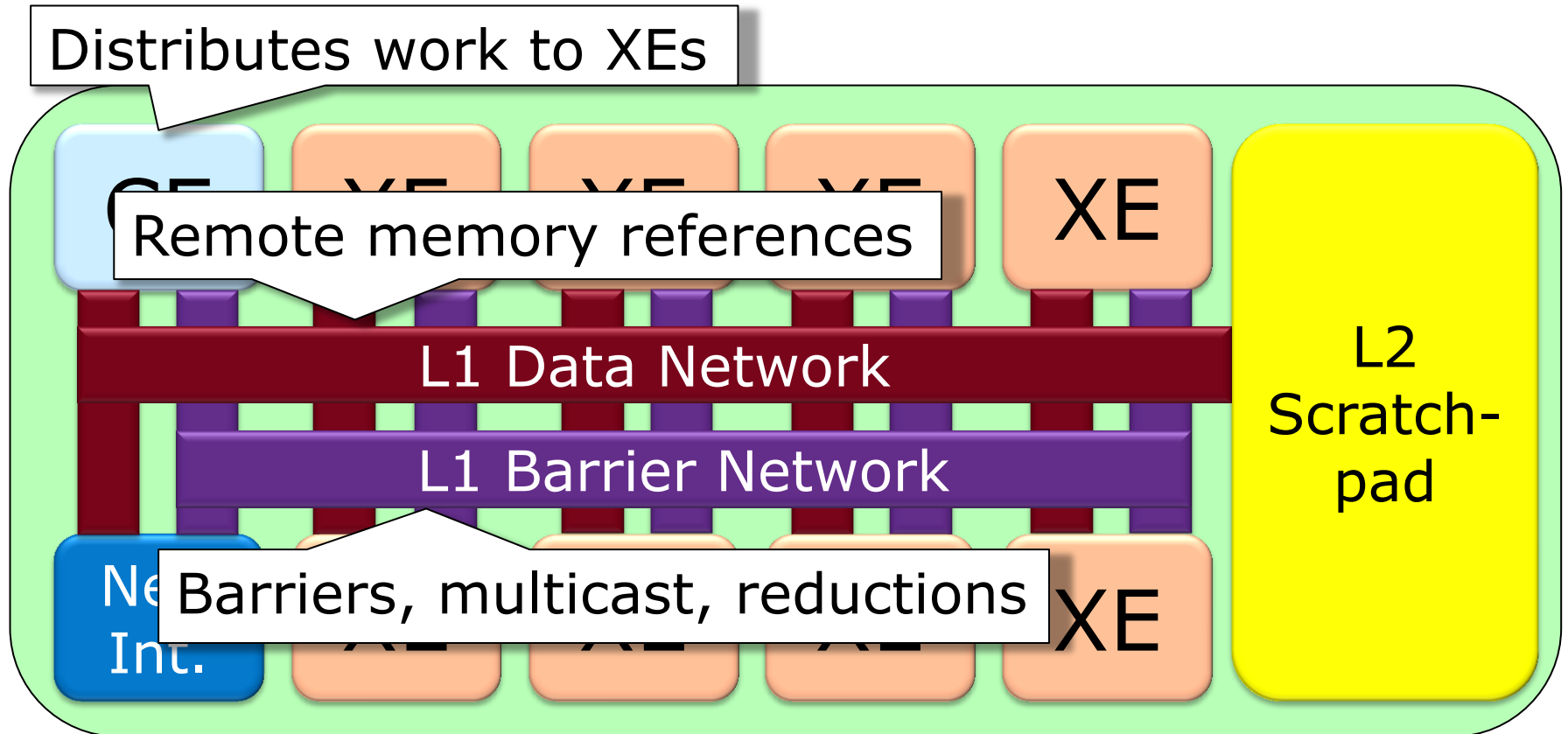


# Blocks: Cores Grouped for Locality



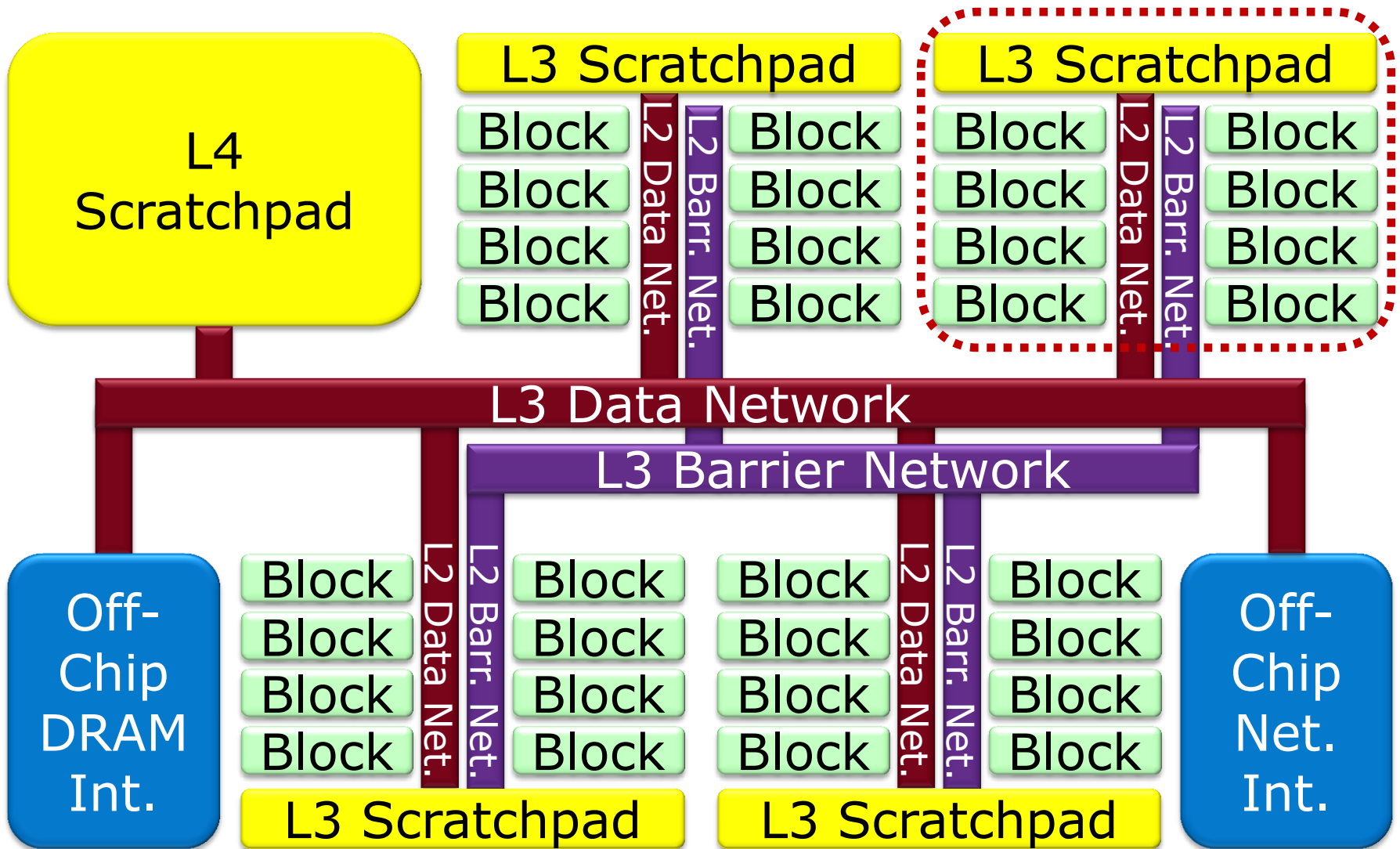


# Blocks: Cores Grouped for Locality



# Runnemeade

Unit



## Case Studies

- Co-design for Synthetic Aperture Radar
- Scratchpads vs. caches
- Network analysis (in paper)

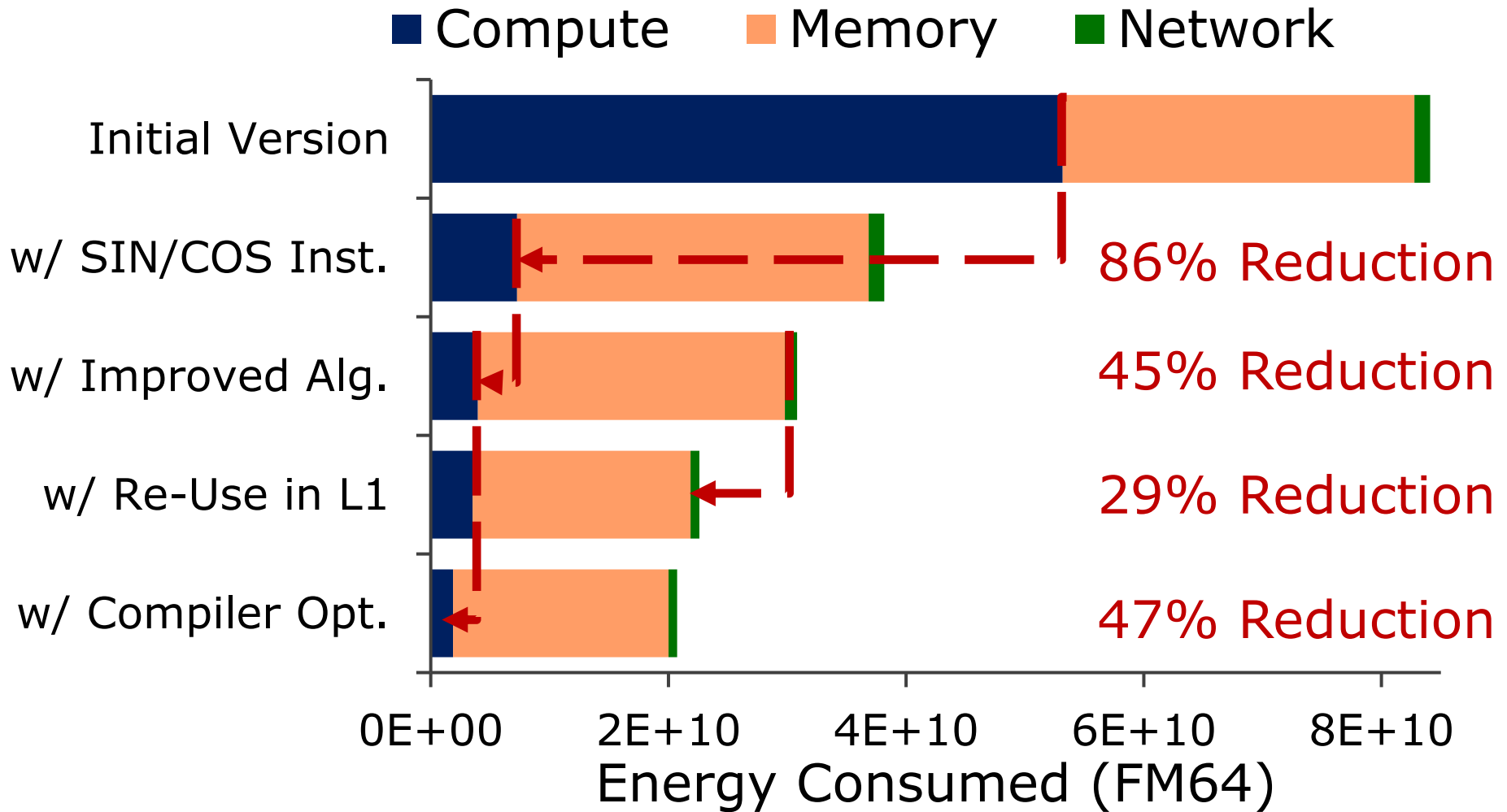
Energy unit: double-precision floating-point multiply (FM64)

# Co-Design for Synthetic Aperture Radar

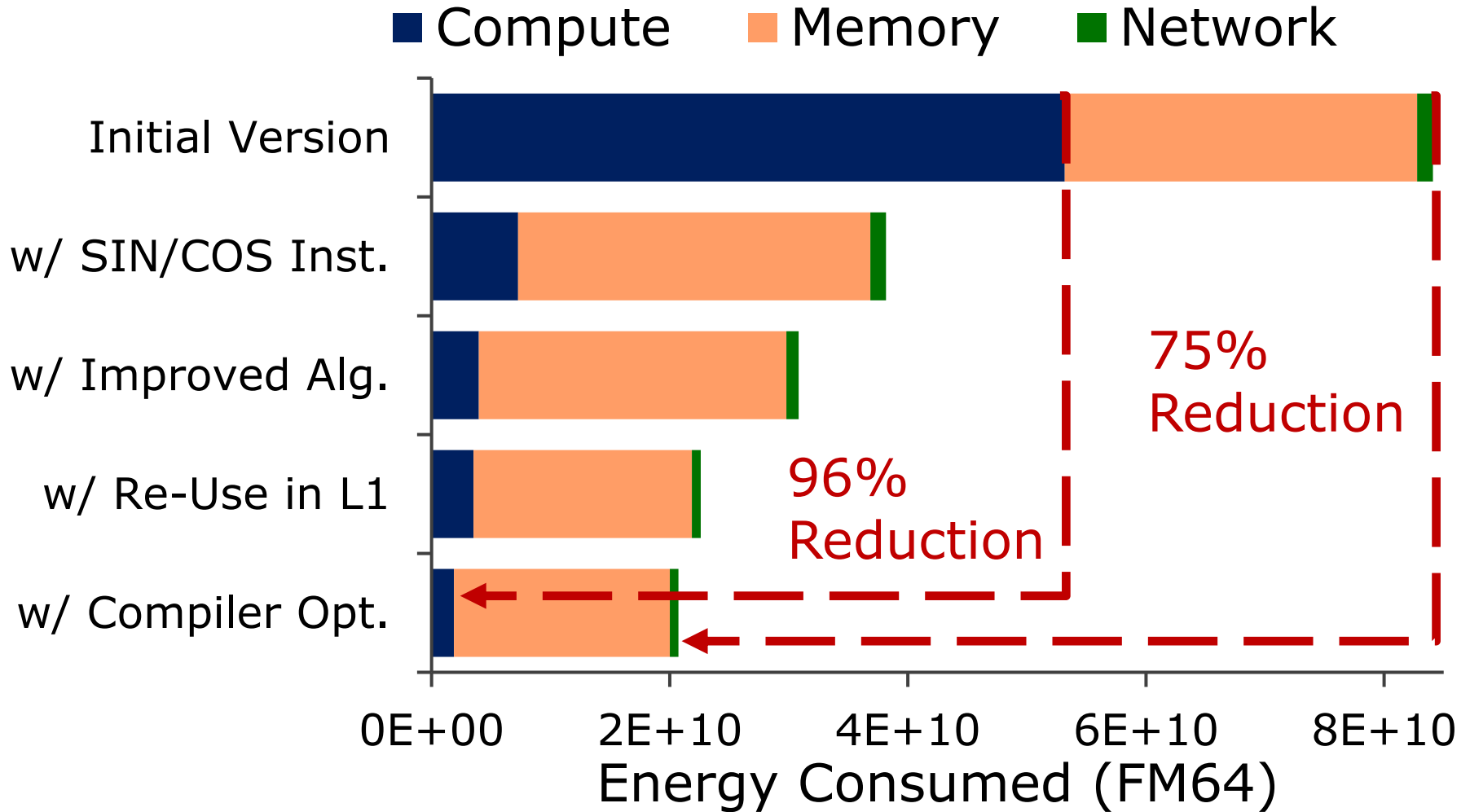
SAR: UHPC “challenge problem”

HW, SW co-designed for energy efficiency

# Codesign for Synthetic Aperture Radar



# Codesign for Synthetic Aperture Radar



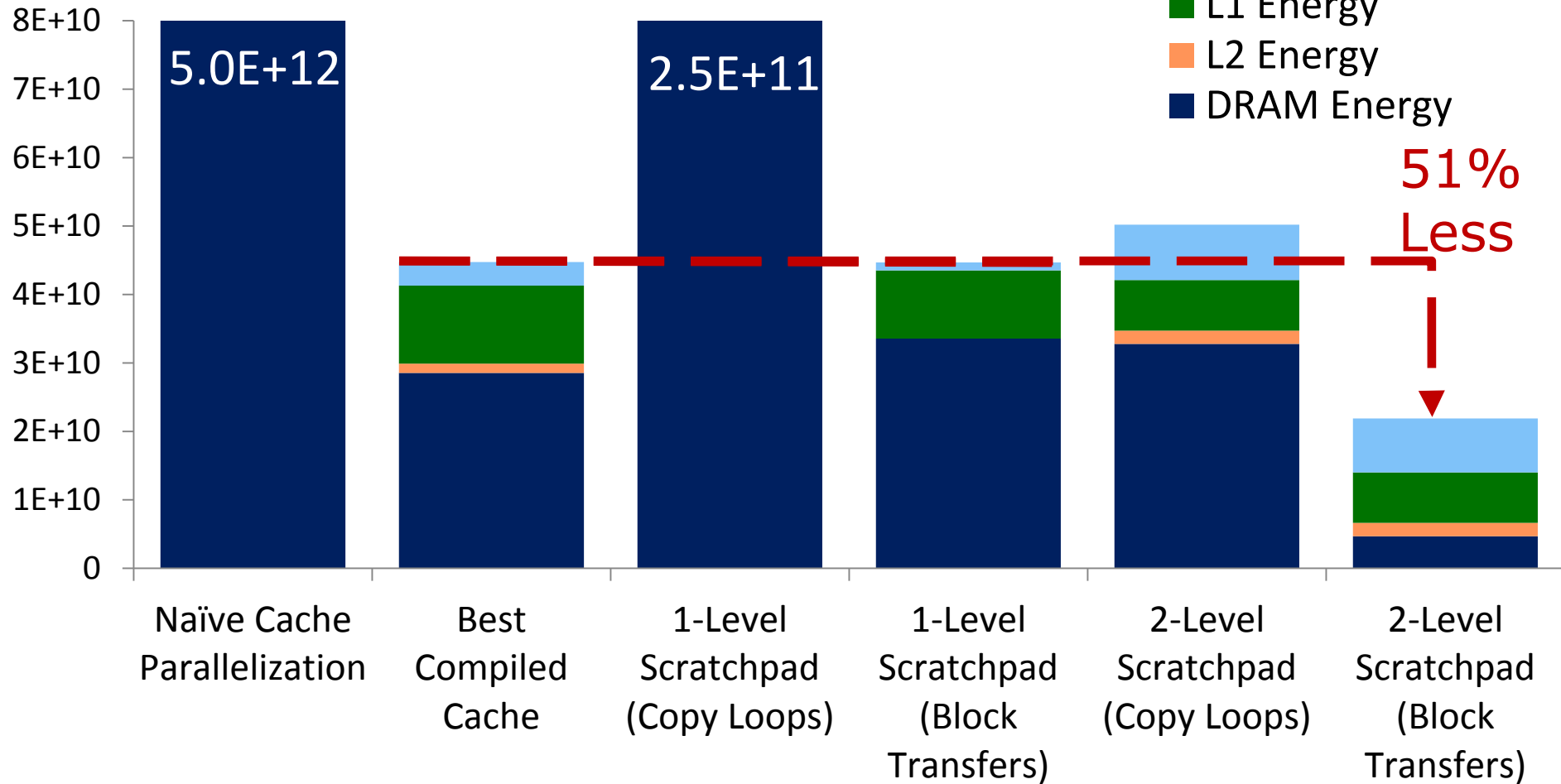
# Comparing Scratchpads and Caches

Questions:

- Energy?
- Programming Effort?

# Matrix Multiplication

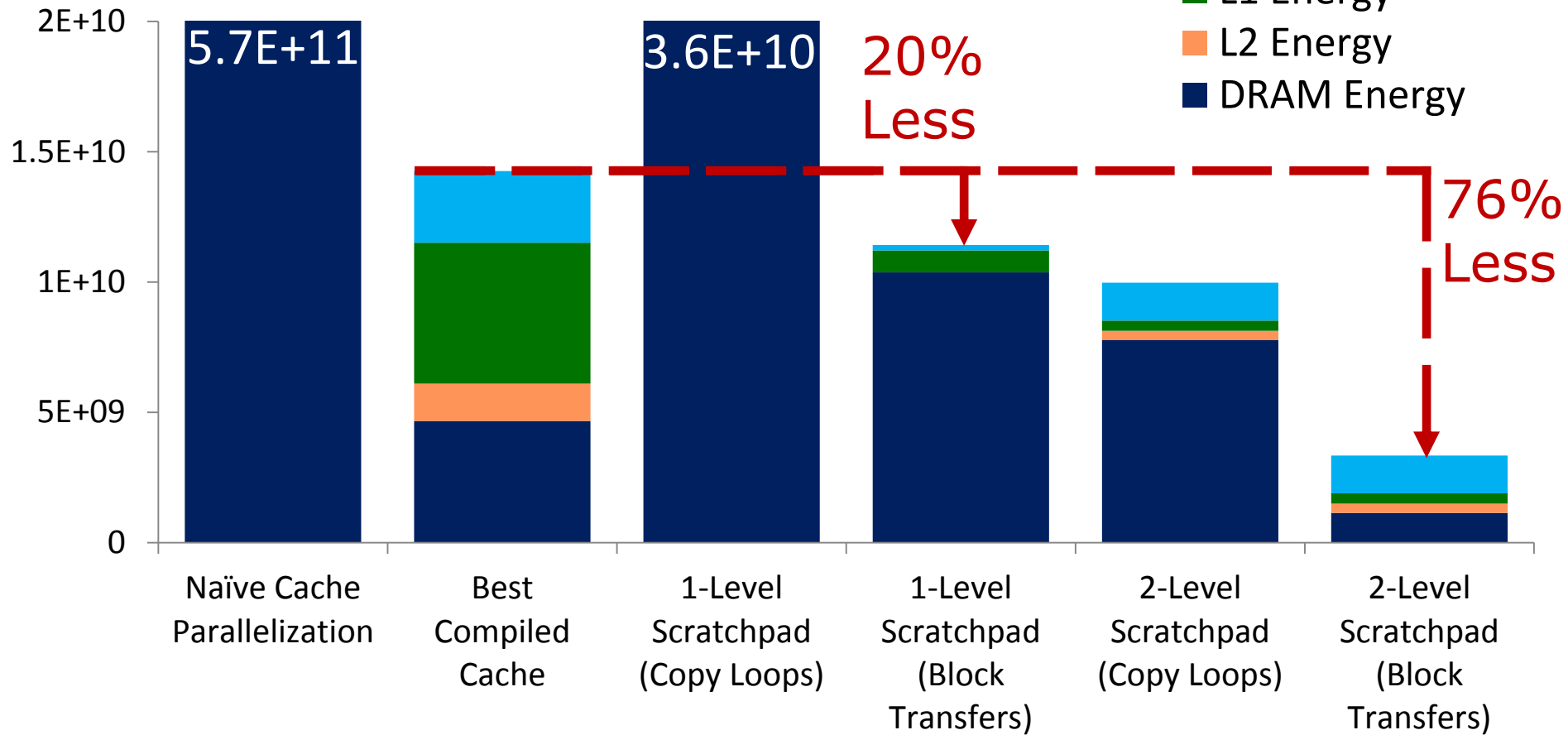
Memory Energy  
(FM64)





# Givens QR Decomposition

Memory Energy  
(FM64)



# Conclusion

Runnemedede is an energy-optimized research architecture

- NTV circuits, power/clock gating, co-design, SW-managed memory
- Co-design: 4x energy improvement
- SW-managed memory: 2-4x memory energy improvement

