A Trace-driven Analysis of Sharing Behavior in TPC-C

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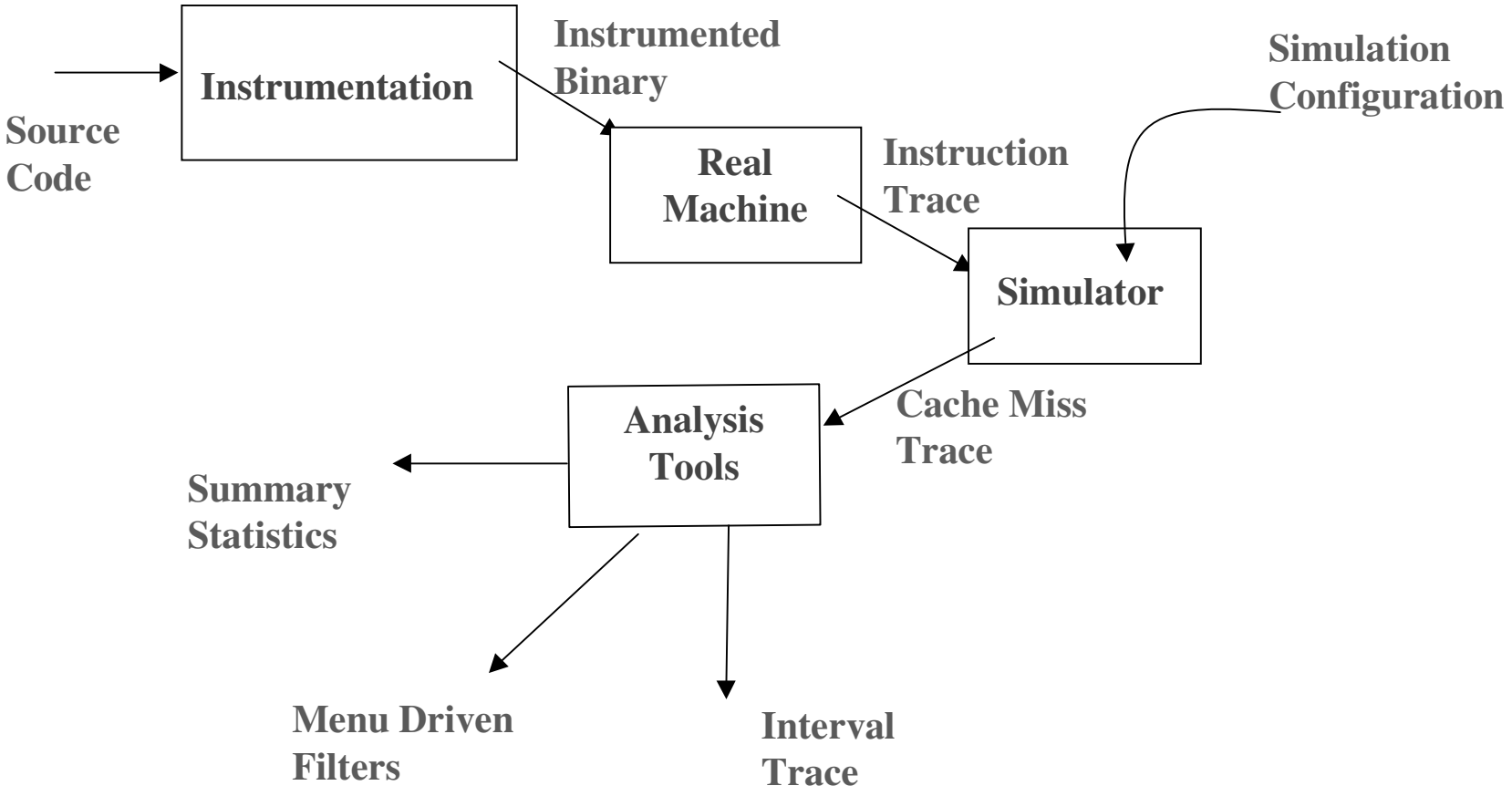
Outline

- Introduction and Motivation
- Trace-Driven Methodology
- Workload Characterization Model
- TPC-C Results and Analysis
- Conclusion

Introduction

- High-End Server Design
  - Rapidly advancing processor technology
  - Memory system is now the bottleneck
- Applications and Workloads
  - Scientific applications have been traditionally used to evaluate improved architectures and protocols
  - Commercial workloads such as OLTP now comprise more than 80% of the high-end server market.
- Increasing need to understand the interaction of commercial workloads and the memory system

Trace Driven Methodology



TPC-C Memory Blocks and Cache Misses

4-Processor system
Cache Line Size: 64 bytes
Cache Size: 1MB, 4MB

Memory Blocks

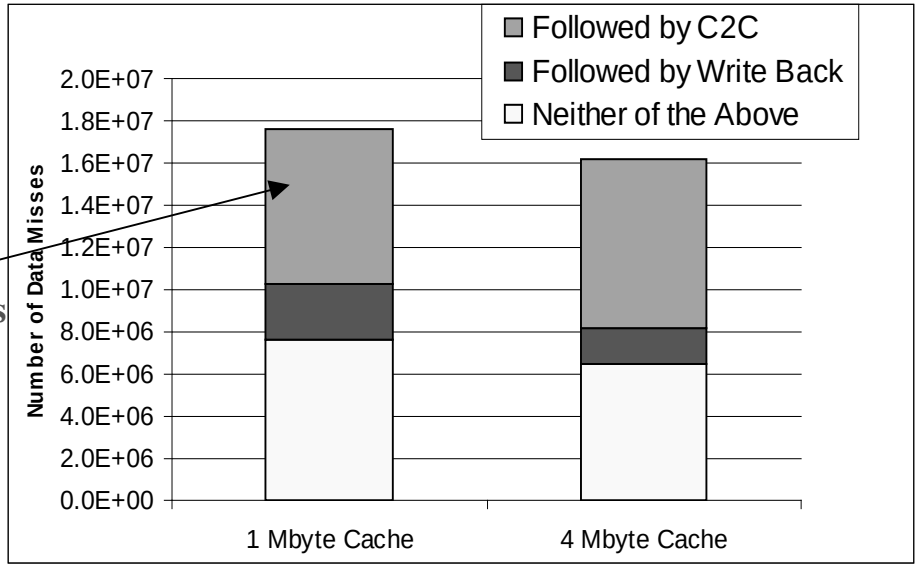
Block Type	Number of Blocks
Total	1,127,551
Code	18,551
Data	1,109,000
Read Only	505,811
Read by All Processors	289,864
Written by All Processors	94,329

Cache Misses

	Number of Misses	
Miss Type	1 Mbyte Cache	4 Mbyte Cache
Total	19,831,481	16,671,364
Code	2,218,711	449,566
Data	17,612,770	16,221,798
Load Data	11,699,004	10,430,401
Store Data	5,913,766	5,791,397

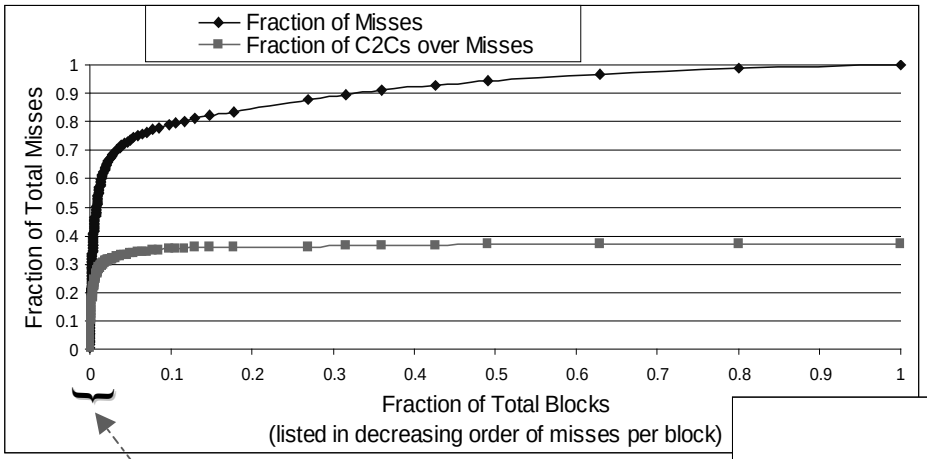
TPC-C Cache-to-Cache Transfers and Write-backs

A large fraction of cache-to-cache transfers



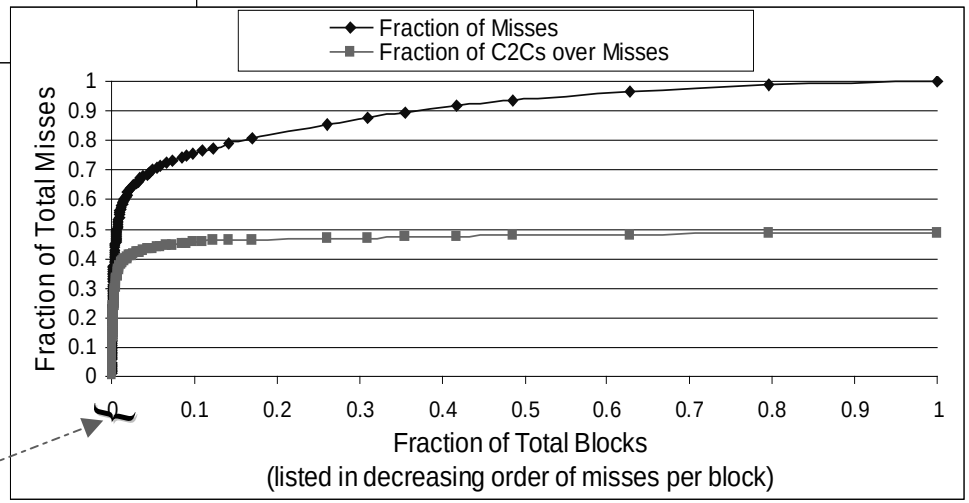
Miss Type	Number of Data Misses	
	1 Mbyte Cache	4 Mbyte Cache
Followed by C2C	7,373,222	8,055,311
Followed by Write Back	2,653,240	1,686,242
Neither of the Above	7,586,308	6,480,245

Breakdown of Misses & C2C transfers by Blocks



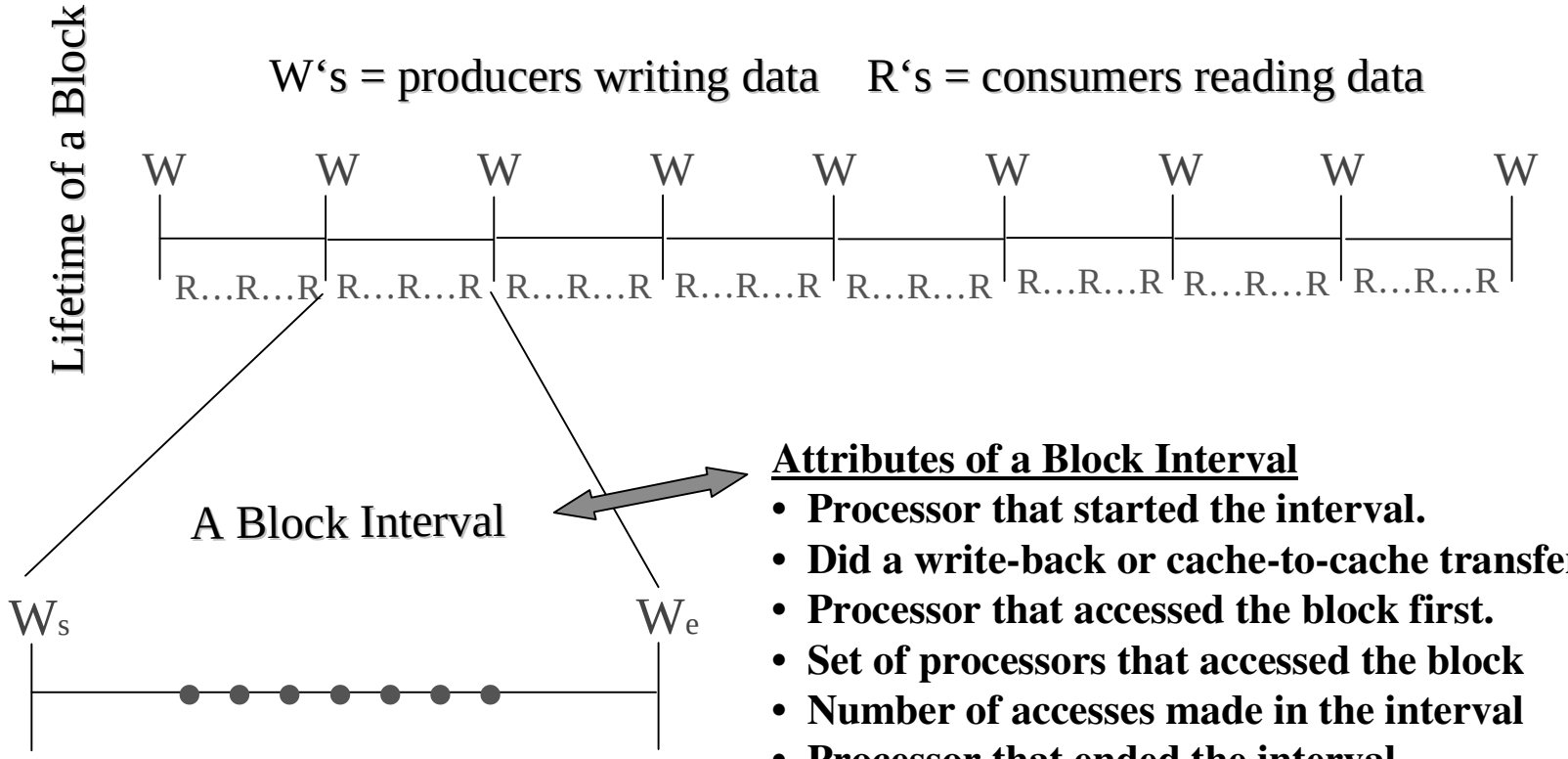
1 Mbyte Cache

4 Mbyte Cache



A small fraction of blocks account for high fraction of misses and C2C transfers

Workload Characterization

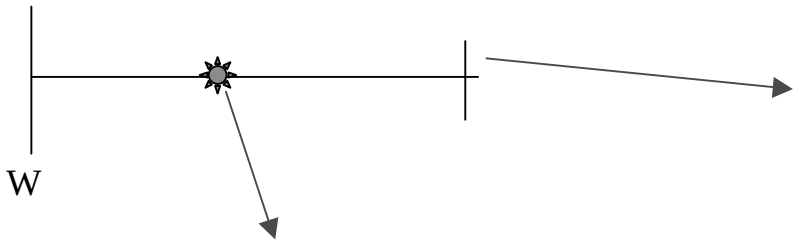


Attributes of a Block Interval

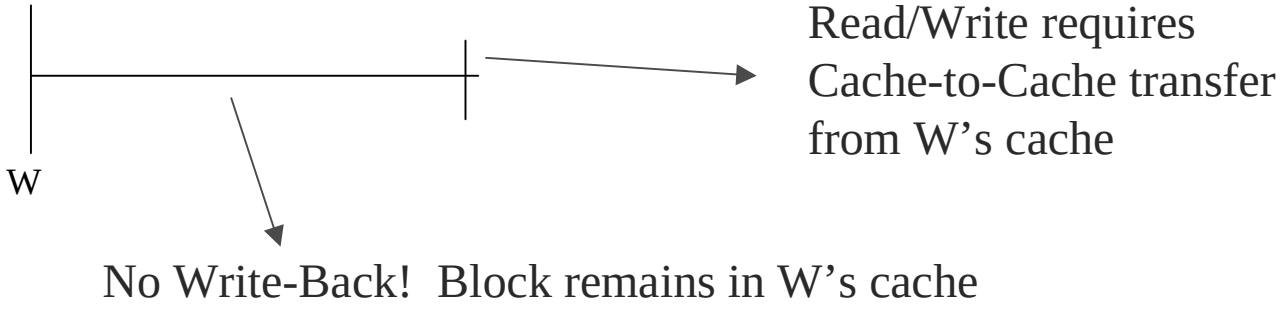
- **Processor that started the interval.**
- **Did a write-back or cache-to-cache transfer occur?**
- **Processor that accessed the block first.**
- **Set of processors that accessed the block**
- **Number of accesses made in the interval**
- **Processor that ended the interval**

Write-Back Intervals vs. Cache-to-Cache Intervals

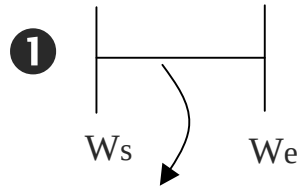
Case 1: A Write-Back Interval (WB-Interval)



Case 2: A Cache-to-Cache Interval (C2C-Interval)

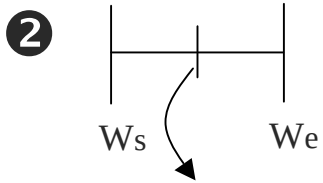


Identifying Sharing Patterns



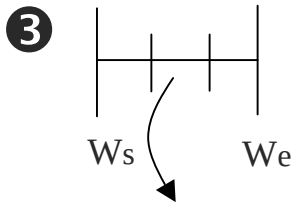
No read misses

Write-After-Write Location Sharing



One read miss

Migratory Sharing Two-Processor Sharing



>= 2 read misses

Producer-Consumer Sharing

Using Filters to Select Blocks

1 Mbyte Cache

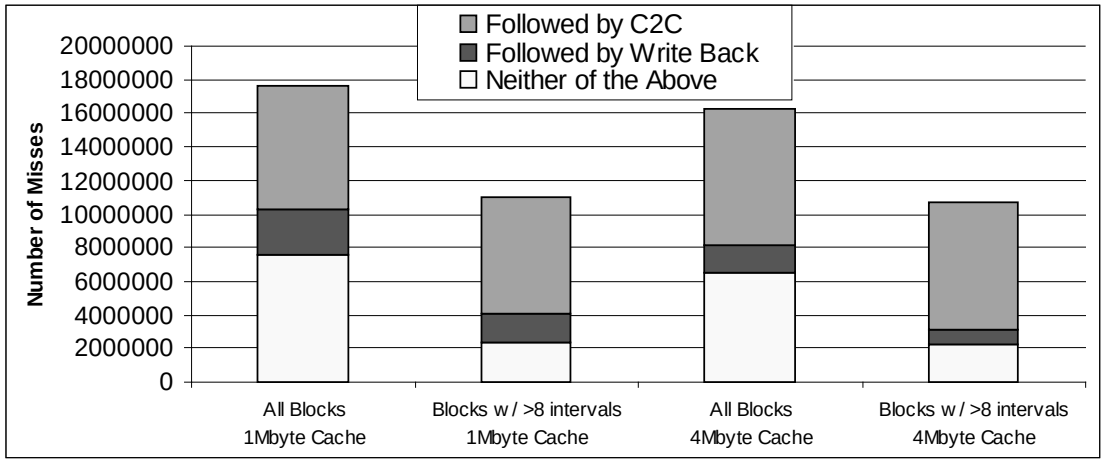
Filter Type	% of Blocks	% of Misses	% of C2Cs
No Filter	100	100	100
> 4 intervals	15.0	59.4	97.8
> 8 intervals	**7.4**	**55.7**	**95.3**
> 16 intervals	4.0	52.5	92.0
> 1024 intervals	0.1	20.9	39.1

4 Mbyte Cache

Filter Type	% of Blocks	% of Misses	% of C2Cs
No Filter	100	100	100
> 4 intervals	14.5	68.0	97.1
> 8 intervals	**7.2**	**63.9**	**94.2**
> 16 intervals	3.9	60.4	90.7
> 1024 intervals	0.1	24.2	36.3

Filtered Sample: 7% blocks account for 55-64% misses and 94-95% C2Cs

Number of Misses
- C2C Transfers
- Write-backs

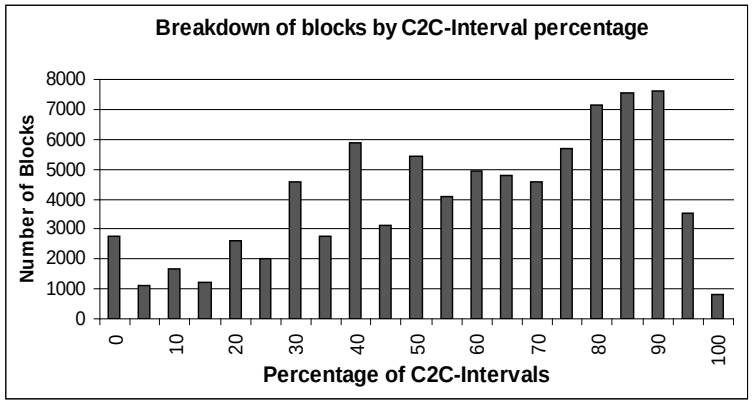


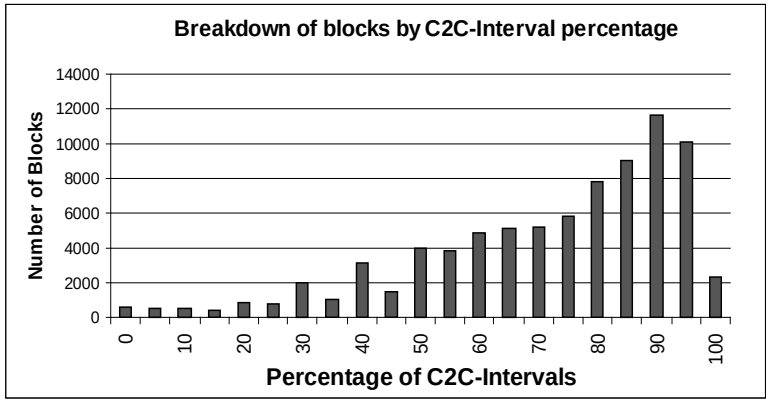
Breakdown of Filtered Blocks and Misses by C2C-Intervals

1 Mbyte Cache

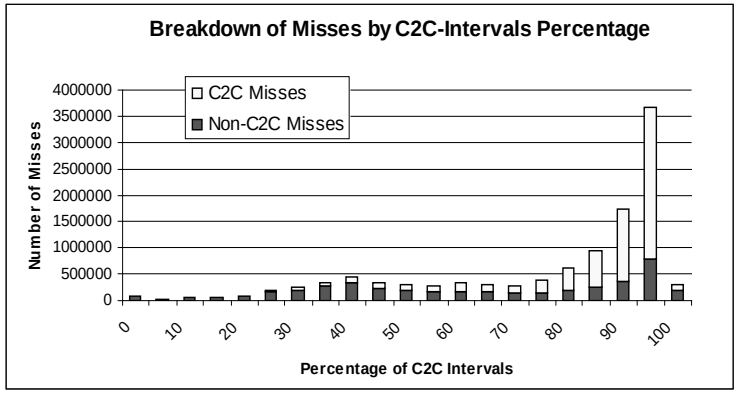
4 Mbyte Cache

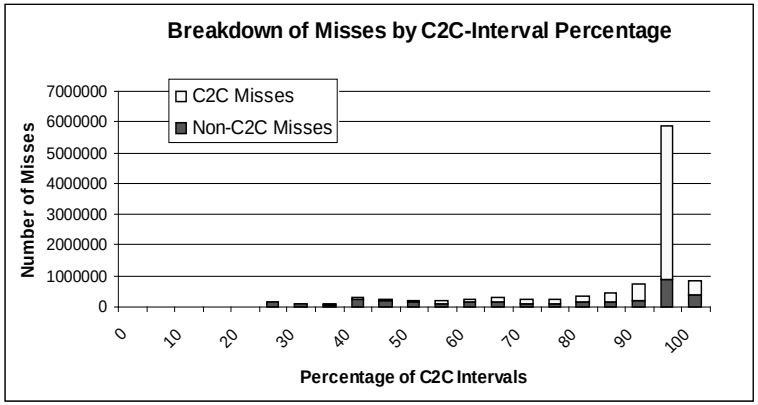
Blocks





Misses

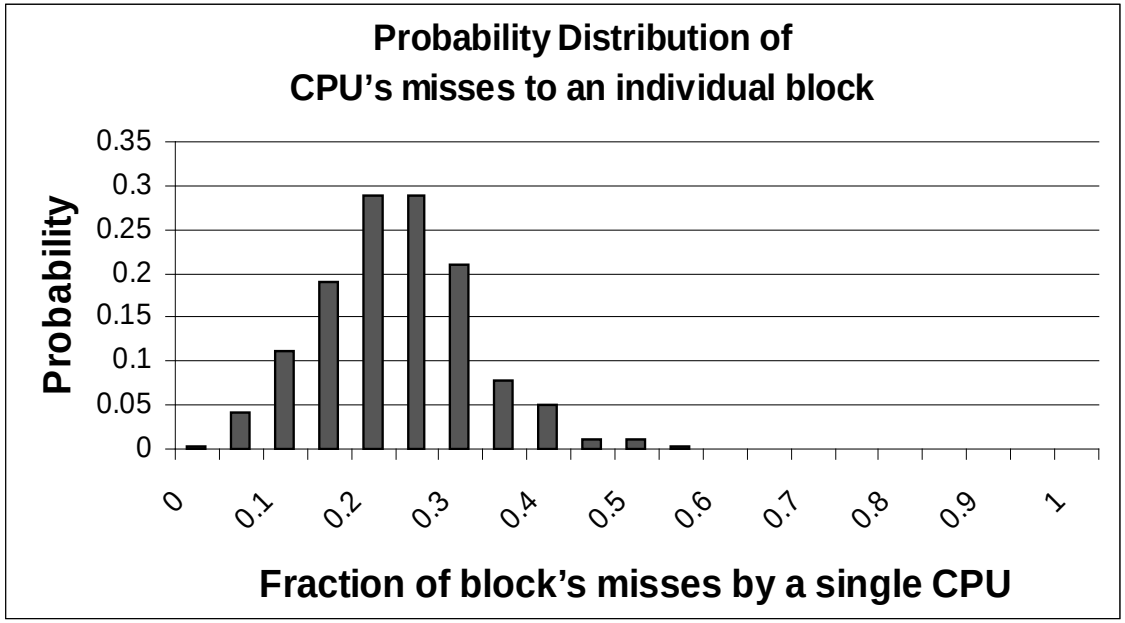




Single CPU Contribution to Misses

64% of the filtered blocks are read and written by all CPUs.
Are misses to any of these blocks dominated by a single CPU?

1 Mbyte Cache



=> High probability that all four CPU's contribute evenly.

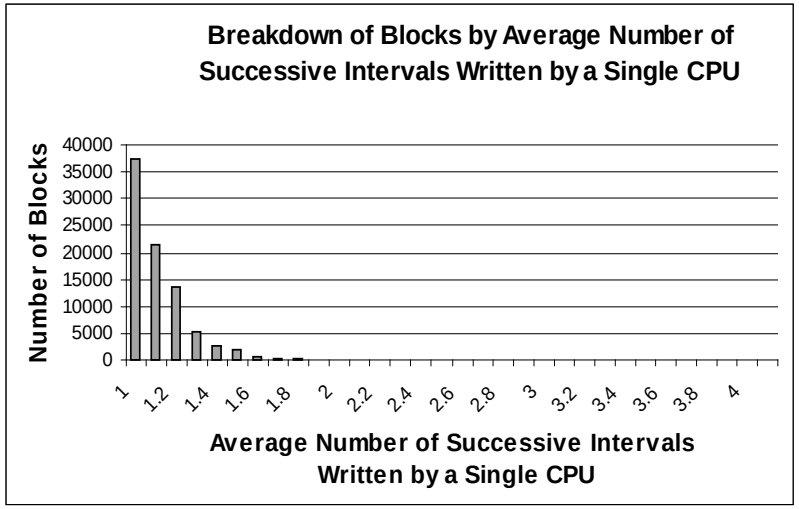
Write Behavior of Filtered Blocks

~92.6% of the filtered blocks are written by all 4 processors.

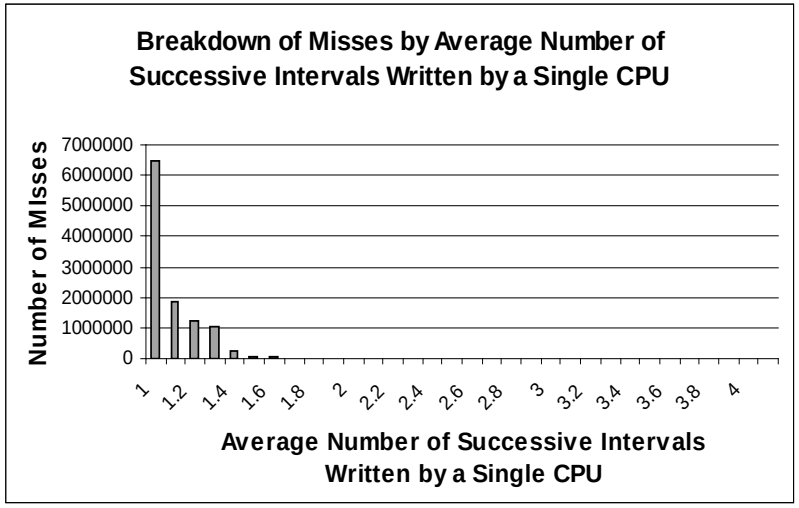
How many successive intervals are written by the same processor?

1 Mbyte Cache

By Blocks



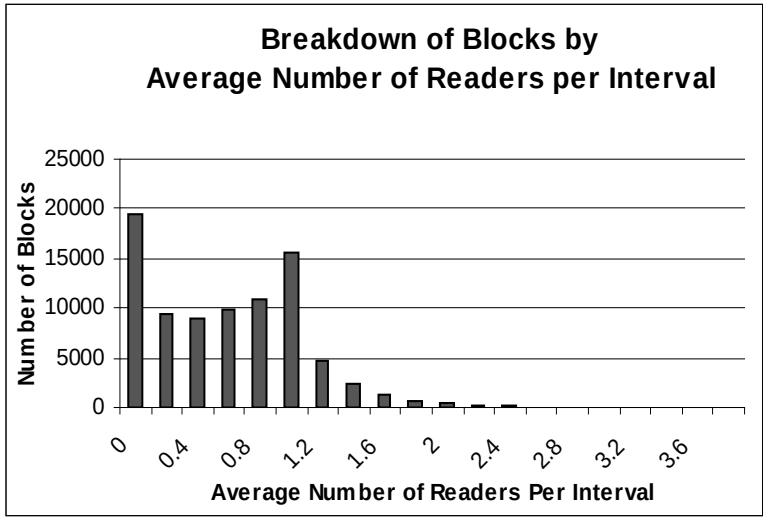
By Misses



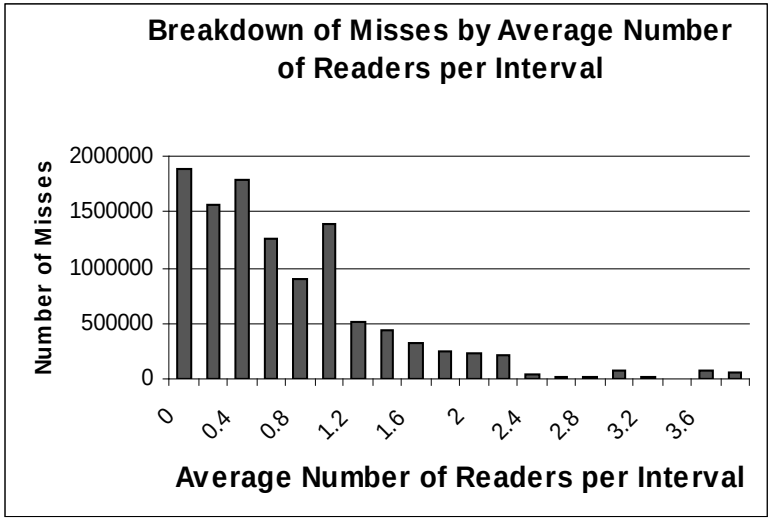
=> High amounts of migratory access patterns

Breakdown of Blocks & Misses by Readers Per Interval

By Blocks



By Misses



=> High amounts of location sharing communication

Summary

- Key Overall Characteristics of TPC-C
  - Data misses outweigh Instruction misses (89% to 11% for 1MB cache)
  - Increasing the size of the cache (1MB to 4MB) reduces the instructions misses considerably (by 80%), but does little for data misses (by 8%)
  - A high fraction (37%-50%) of the misses require cache-to-cache transfers

- Using intervals and filters to characterize and analyze the lifetime of memory blocks.
  - A low fraction of blocks (w/ greater than 8 intervals) account for a high fraction of misses and C2C transfers

- Sharing Characteristics of TPC-C
  - A high fraction of C2C intervals for the filtered sample
  - Location sharing and migratory access patterns
  - High probability of equal CPU participation for block access